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MODEL DQ142
MAGNETIC TAPE COUPLER
INSTRUCTION MANUAL

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DISTRIBUTED LOGIC CORPORATION
1555 S. Sinclair Street
P.O. Box 6270
Anaheim, California 92806
Telephone: (714) 937-5700
Telex: 6836051

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

Section **Page**

ILLUSTRATIONS

TABLES

SECTION 1
DESCRIPTION

INTRODUCTION

This manual describes the installation, operation, programming, troubleshooting and theory of operation of Distributed Logic Corporation (DILOG) Model DQ142 Magnetic Tape Coupler. The coupler interfaces DEC* LSI-11 based computer systems to Industry-Standard formatted magnetic tape drives. The complete coupler occupies one quad module in the backplane. The coupler emulates DEC TS11, TU80 and TSV05 tape subsystems.

COUPLER CHARACTERISTICS

A magnetic tape subsystem consists of a coupler, a formatter and up to four tape drives. The function of the coupler is to buffer data and status between the I/O bus and the formatter and to transfer commands from the I/O bus to the formatter. The formatter, which is embedded in the drive, establishes the data format, controls tape motion and performs error checking. The overall tape control function is a combination of the coupler functions, which are related to the LSI-11, and formatter functions, which are related to the tape drives. Figures 1-1 and 1-2 are simplified diagrams of magnetic tape systems.

A microprocessor is the sequence and timing center of the coupler. The control information is stored as firmware instructions in Read Only Memory (ROM) on the coupler board. One section of the ROM contains a diagnostic program that tests the functional operation of the coupler. This self test is performed automatically each time power is applied or whenever a diagnostic command is issued. A green diagnostic indicator on the board lights if self test passes. If self test fails, the coupler has an automatic data feature that stops the computer from interacting with the tape formatter and thus prevents writing erroneous information into critical data base areas.

LSI-11 Q BUS INTERFACE

Commands, data and status transfers between the coupler and the computer are executed via the parallel I/O bus (Q Bus) of the computer directly to memory, via the DMA facility of the Q Bus. Coupler/Q Bus interface signals are listed in Table 1-1.

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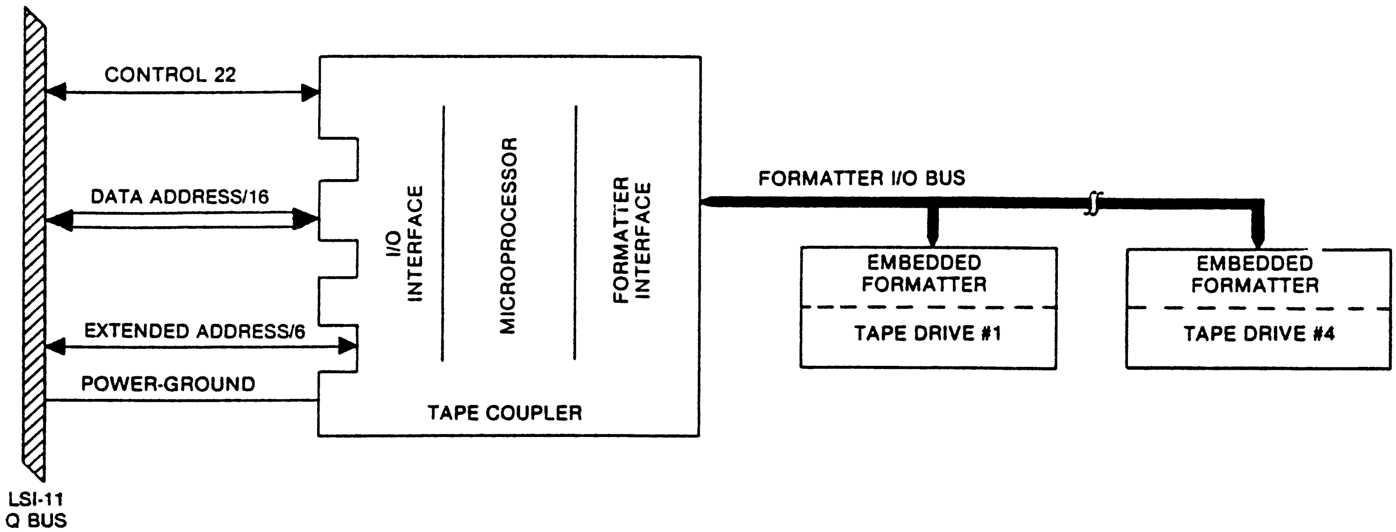


Figure 1-1. Tape System (Maximum Configuration) Four Embedded Formatter Tape Drives

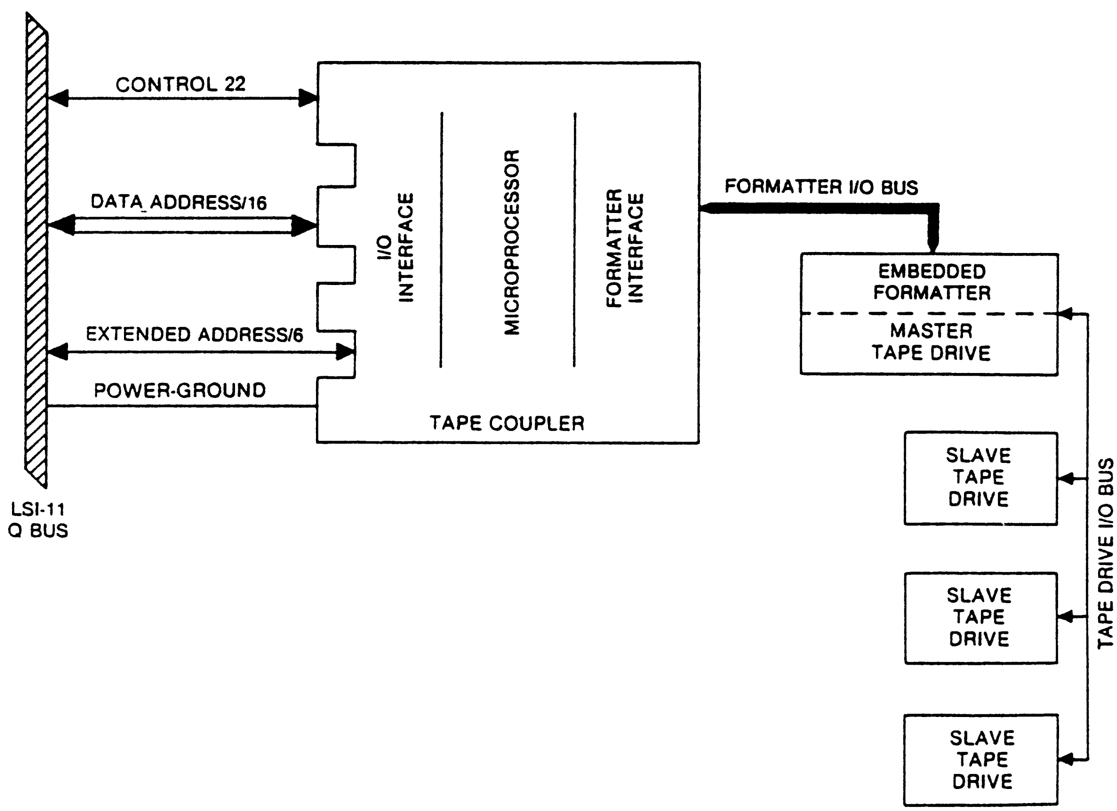


Figure 1-2. Tape System (Maximum Configuration) One Embedded Formatter Tape Drive with Three Slave Tape Drives

Table 1-1. Coupler/Q Bus Interface Lines

Bus Pin	Mnemonic	Controller Input/ Output	Description
AJ1, AM1, RT1, BJ1, BM1, BT1, BC2, CJ1, CM1, CT1, CC2, DJ1, DM1, DT1, DC2	GND	O	Signal Ground and DC return.
AN1	BDMR L	O	Direct Memory Access (DMA) request from controller: active low.
AP1	BHALT L	N/A	Stops program execution. Refresh and DMA is enabled. Console operation is enabled.
AR1	BREF L	N/A	Memory Refresh.
BA1	BDCOK H	I	DC power OK. All DC voltages are normal.
BB1	BPOK H	N/A	Primary power OK. When low activates power fail trap sequence.
BN1	BSACK L	O	Select Acknowledge. Interlocked with BDMGO indicating controller is bus master in a DMA sequence.
BR1	BEVNT L	N/A	External Event Interrupt Request.
BV1, AA2, BA2, CA2, DA2	+5	I	+5 volt system power.
AD2, BD2	+12	N/A	+12 volt system power.
AE2	BDOUT L	I/O	Data Out. Valid data from bus master is on the bus. Interlocked with BRPLY.
AF2	BRPLY L	I/O	Reply from slave to BDOUT or BDIN and during IAK.
AH2	BDIN L	I/O	Data Input. Input transfer to master (states master is ready for data). Interlocked with BRPLY.
AJ2	BSYNC L	I/O	Synchronize: becomes active when master places address on bus; stays active during transfer.
AK2	BWTBT L	I/O	Write Byte: indicates output sequence to follow (DATO or DATOB) or marks byte address time during a DATOB.
AL2	BIRQ L	O	Interrupt Request.
AM2 AN2 CM2 CN2	BIAK1I L BIAK1O L BIAK2I L BIAK2O L	I O I O	Serial Interrupt Acknowledge input and output lines routed from Q Bus, through devices, and back to processor to establish an interrupt priority chain.
AT2	BINIT L	I	Initialize. Clears devices on I/O bus.
AU2, AV2, BE2, BF2, BH2, BJ2, BK2, BL2, BM2, BN2, BP2, BR2, BS2, BT2, BU2, BV2	BDAL0 L through BDAL15 L	I/O	Data/address lines, 0-15.
AR2 AS2 CR2 CS2	BDMG1I L BDMG1O L BDMG2I L BDMG2O L	I O I O	DMA Grant Input and Output. Serial DMA priority line from computer, through devices, and back to computer.
AP2	BBS7 L	I	Bank 7 Select. Asserted by bus master when address in upper 4K bank is placed on the bus.
AC1, AD1, BC1, BD1, BE1, BF1	BDAL 16 L -BDAL 21 L	O	Extended Address Bits 16-21.

FORMATTER INTERFACE

The coupler interfaces with the formatted tape drives through two 50-pin flat cable connectors at the top of the coupler board. The maximum cable length between coupler and formatter is 25 feet. Coupler/formatter interface signals are listed in Tables 1-2 and 1-3.

Table 1-4 lists the manufacturers and connector correlations.

COUPLER SPECIFICATIONS

Data Format
- Industry standard non-return-to-zero (NRZ), Phase Encoded (PE), or Group Coded Recording (GCR) recording.
- 9 tracks.
- Recording densities:
  800 characters per inch (NRZ)
  1600 characters per inch (PE)
  6250 characters per inch (GCR)
- Inter-record Gap (IRG) = 0.50 inch min. (NRZI/PE) or 0.30 inch min. (GCR)

Media Characteristics
- Type:
  ½" wide mylar base, oxide coated, magnetic tape.
- Reel Size:
  7", 8½", or 10½" diameter tape reels containing 600, 1,200 and 2,400 feet of tape, respectively.
- Data Capacity (megabytes):
  Assumes approximately 80% recording efficiency:

		800 CPI	1600 CPI	6250 CPI
600 Ft.	=	5.75	11.5	
1,200 Ft.	=	11.5	23.0	
2,400 Ft.	=	22.0	44.0	172.0

- Data Transfer Rate (Characters/Second):

		800 CPI	1600 CPI	6250 CPI
12.5 ips	=	10,000	20,000	
25.0 ips	=	20,000	40,000	
37.5 ips	=	30,000	60,000	
45.0 ips	=	36,000	72,000	280,000
75.0 ips	=	60,000	120,000	470,000
125.0 ips	=	100,000	200,000	780,000

Emulation:
- TS11, TU80, TSV05

Register Address:
- Data/Address Buffer (TSDB/TSBA) 772 520*
- Status (TSSR) 772 522*
- Extended Data Buffer (TSDBX) 772 523

*Addresses are for first unit; addresses for successive units are Modulo four higher than next-lower numbered unit. Alternate addresses are jumper-selectable.

Computer I/O Interface:
- Interrupt Vector Address 224 (first unit) Alternate Address switch selctable; switch-selectable for successive units.
- Priority Level BR4 (jumper-selectable).
- DMA data transfers.
- Packet Processing type programming.
- One std. bus load.

Addressable Memory:
- Switch-selectable: 18/22 bits (256KB/4.0MB)

Coupler Formatter Interface:
- Coupler is compatible with tape formatters manufactured by CDC, Cipher, Digi-Data, Kennedy, Pertec, Ampex, S.E. Labs, Thorn Data, STC, Fujitsu.

Packaging
- The coupler is completely contained on one quad module 10.44 inches (26.51 cm) by 8.88 inches (22.55 cm).

Documentation:
- One Instruction Manual is supplied with the coupler.

Power:
- +5, ±0.25 VDC at 4.0 amps, from computer backplane.

Environment:
- Operating temperature 50°F (10°C) to 140°F (60°C). Operating humidity 10% to 95% non-condensing.
  NOTE: The quality of recording and reading information on magnetic tape is affected by temperature and humidity. The environment where the tape is used should be maintained within the following limits:
  Temperature: 60°F (15°C) to 85°F (32°C)
  Humidity: 20% to 80% non-condensing

Shipping Weight:
- Five pounds including documentation.

Table 1-2. Coupler Connector J1 to Formatter Interface Lines

J1 Signal	J1 Return	Mnemonic	Description
2	1	FFBY	Formatter Busy
4	3	FLWD	Last Word
6	5	FWD4	Write Data 4
8	7	FGO	Initiate Command
10	9	FWD0	Write Data 0
12	11	FWD1	Write Data 1
14	13		Not Used
16	15	FLOL	Load on Line
18	17	FREV	Reverse/Forward
20	19	FREW	Rewind
22	21	FWDP	Write Data Parity
24	23	FWD7	Write Data 7
26	25	FWD3	Write Data 3
28	27	FWD6	Write Data 6
30	29	FWD2	Write Data 2
32	31	FWD5	Write Data 5
34	33	FWRT	Write/Read
36	35	FRTH2 (FLGAP)	Read Threshold 2
38	37	FEDIT	Edit
40	39	FERASE	Erase
42	41	FWFM	Write File Mark
44	43	FRTH1 (SPARE)	Read Threshold 1
46	45	FTAD0	Transport Address 0
48	47	FRD2	Read Data 2
50	49	FRD3	Read Data 3

Note: ( ) Parentheses are applicable to streaming and GCR drives.

Table 1-3. Coupler Connector J2 Formatter Interface Lines

J2 Signal	J2 Return	Mnemonic	Description
1		FRDP	Read Data Parity
2		FRD0	Read Data 0
3		FRD1	Read Data 1
4		FLDP	Load Point
6	5	FRD4	Read Data 4
8	7	FRD7	Read Data 7
10	9	FRD6	Read Data 5
12	11	FHER	Hard Error
14	13	FFMK	File Mark
16	15	FCCG/ID	CCG/IDENT
18	17	FFEN	Formatter Enable
20	19	FRD5	Read Data 5
22	21	FEOT	End of Tape
24	23	FOFL	Off Line
26	25	FNRZ (FGOR)	NRZI (GCR) status
28	27	FRDY	Ready
30	29	FRWD	Rewinding
32		FFPT	File Protect
34	33	FRSTR	Read Strobe
36	35	FDWDS	Demand Write Data Strobe
38	37	FDBY	Data Busy
40	39	(FHSPD)	High Speed Status
42	41	FCER	Corrected Error
44	43	FONL	On-Line
46	45	FTAD1	Transport Address 1
48	47	FFAD	Formatter Address
50	49	FDEN (FHISD)	Speed/Density Select

Note: ( ) Parentheses are applicable to streaming and GCR drives.

Table 1-4. Coupler to Formatter Connection Correlation

Coupler Connector J1 to:

Manufacturer	Model	Connector
CDC	Keystone II, 92180, 92181	J4
Cipher	F880, M89X, M99X	P1
	F100X, F900X (Adapter required)	P4
Digi-Data	Formatted	JC
Fujitsu	M244X	JA
IDT	1012	J1
	1050	J124
Kennedy	6809 Streamer	J1
	Formatted	
Pertec	Formatted (Embedded)	P4
	External Formatter (Adapter required)	P4
STC	2921/2	J7

Coupler Connector J2 to:

Manufacturer	Model	Connector
CDC	Keystone II, 92180, 92181	J5
Cipher	F880, M89X, M99X	P2
	F100X, F900X (Adapter required)	P5
Digi-Data	Formatted	JD
Fujitsu	M244X	JB
IDT	1012	J2
	1050	J125
Kennedy	6809 Streamer	J1
	Formatted	J1
Pertec	Formatted (Embedded)	P5
	External Formatter (Adapter required)	P5
STC	2921/2	J6

BLANK

SECTION 2
INSTALLATION

INSPECTION

The padded shipping carton that contains the coupler board also contains an instruction manual and cables to the mag tape drives (if this option is exercised). The coupler is completely contained on the quad-size printed circuit board. The drive (or drives), if supplied, is contained in a separate shipping carton. Inspect the coupler and cable(s) for damage.

CAUTION

If damage to any of the components is noted, do not install. Immediately inform the carrier and DILOG.

Installation instructions for the tape drive are contained in the tape drive manual. Before installing any components of the mag tape system, read Sections 1, 2 and 3 of this manual. Figure 2-1 illustrates the configuration of the coupler.

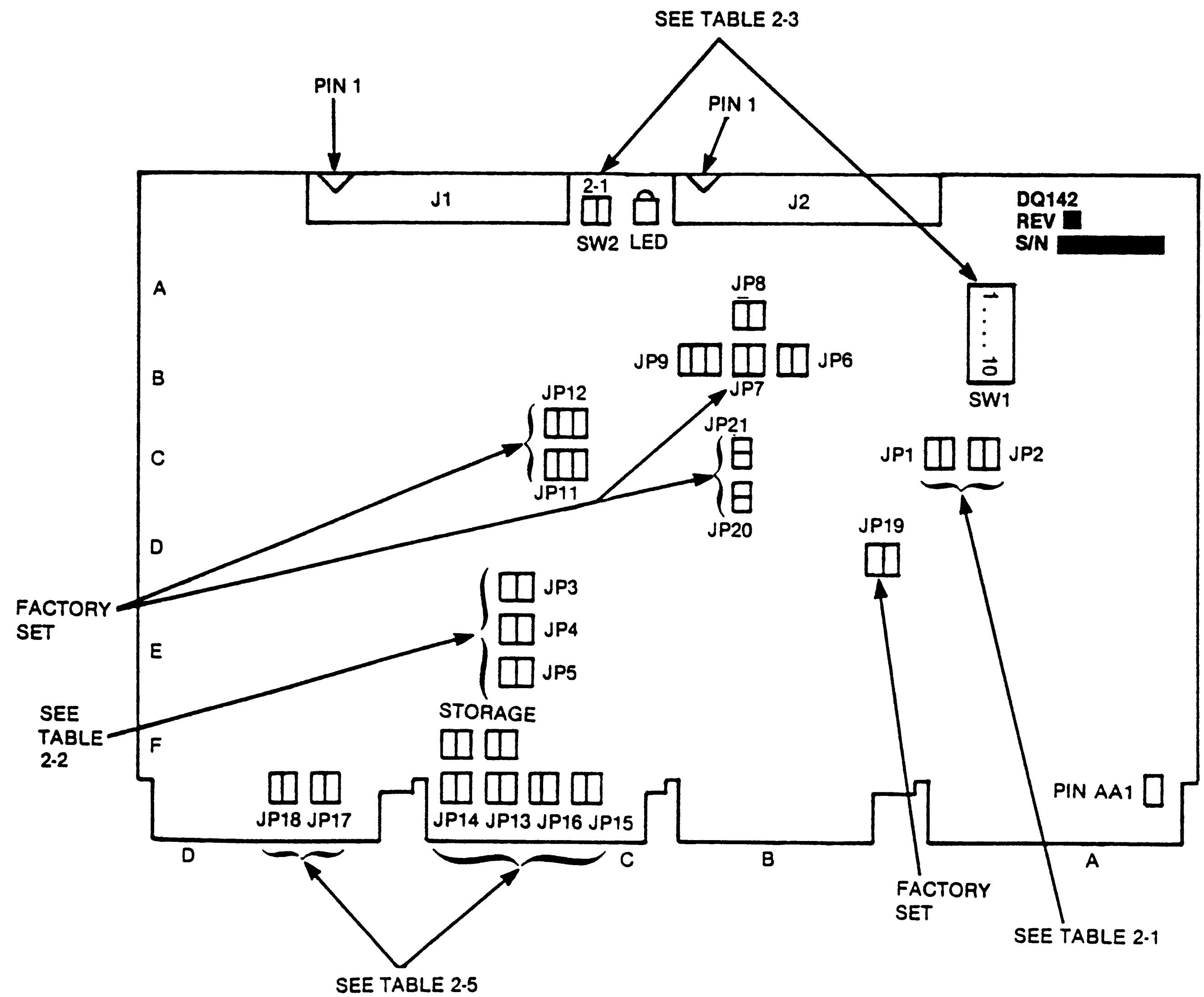


Figure 2-1. Coupler Configuration

PRE-INSTALLATION CHECKS

There are various LSI-11 configurations for LSI-11 based systems. Certain configurations require minor modifications before operating the mag tape system. These modifications are as follows:

A. If the system contains a REV11-C module, it must be placed closer to the processor module (higher priority) than the coupler if the DMA refresh logic on the REV11-C is enabled.

B. If the 4K memory on the DK11-F is not used and the memory in the system does not require external refresh, the DMA refresh logic on the REV11-C should be disabled by removing jumper W2 on the REV11-C module.

C. If the system contains a REV11-A module, the refresh DMA logic must be disabled since the module must be placed at the end of the bus (REV11-A contains bus terminator).

D. If the REV11-C module is installed, cut the etch to pin 12 on circuit D30 (top of board) and add a jumper between pin 12 and pin 13 of D30.

E. If the system requires more than one backplane, place the REV-11 terminator in the last available location in the last backplane.

Be sure to read "Configuring the coupler" paragraph of this section before installation.

INSTALLATION

To install the coupler module, proceed as follows:

CAUTION

Remove DC power from mounting assembly before inserting or removing the coupler module.

Damage to the backplane assembly may occur if the coupler module is plugged in backwards.

1. Select the backplane location into which the coupler is to be inserted.

   There are several backplane assemblies available from DEC and other manufacturers. Figure 2-2 shows typical backplane configurations. Note that the processor module is always installed in the first location of the backplane or in the first location in the first backplane of multiple backplane systems.

   It is important that all option slots between the processor and the coupler be filled to ensure that the daisy chained interrupt (BIAK) and DMA (BDMG) signal be complete to the coupler slots. If there must be empty slots between the coupler and any option board, the following backplane jumpers must be installed:

FROM	TO	SIGNAL
C0 × NS	C0 × M2	BIAK1/L0
C0 × S2	C0 × R2	BDMG1/L0
↑ Last Full Option Slot	↑ Coupler Slot	

2. Insert the coupler into the selected backplane position. Be sure the coupler is installed with the components facing row one, the processor.

   The coupler module is equipped with handles on the side opposite the slot connectors. Gently position the module slot connectors into the backplane then press until the module connectors are firmly seated into the backplane. Both handles must be pressed simultaneously. When removing the module, apply equal pulling pressure to both handles.

3. Feed the module connector end of the tape drive cable(s) into the coupler module connector(s). Install the cable connector(s) into the module connector(s). Verify that the connector(s) are firmly seated.

4. Connect the drive end of the I/O cables to the drive I/O connectors.

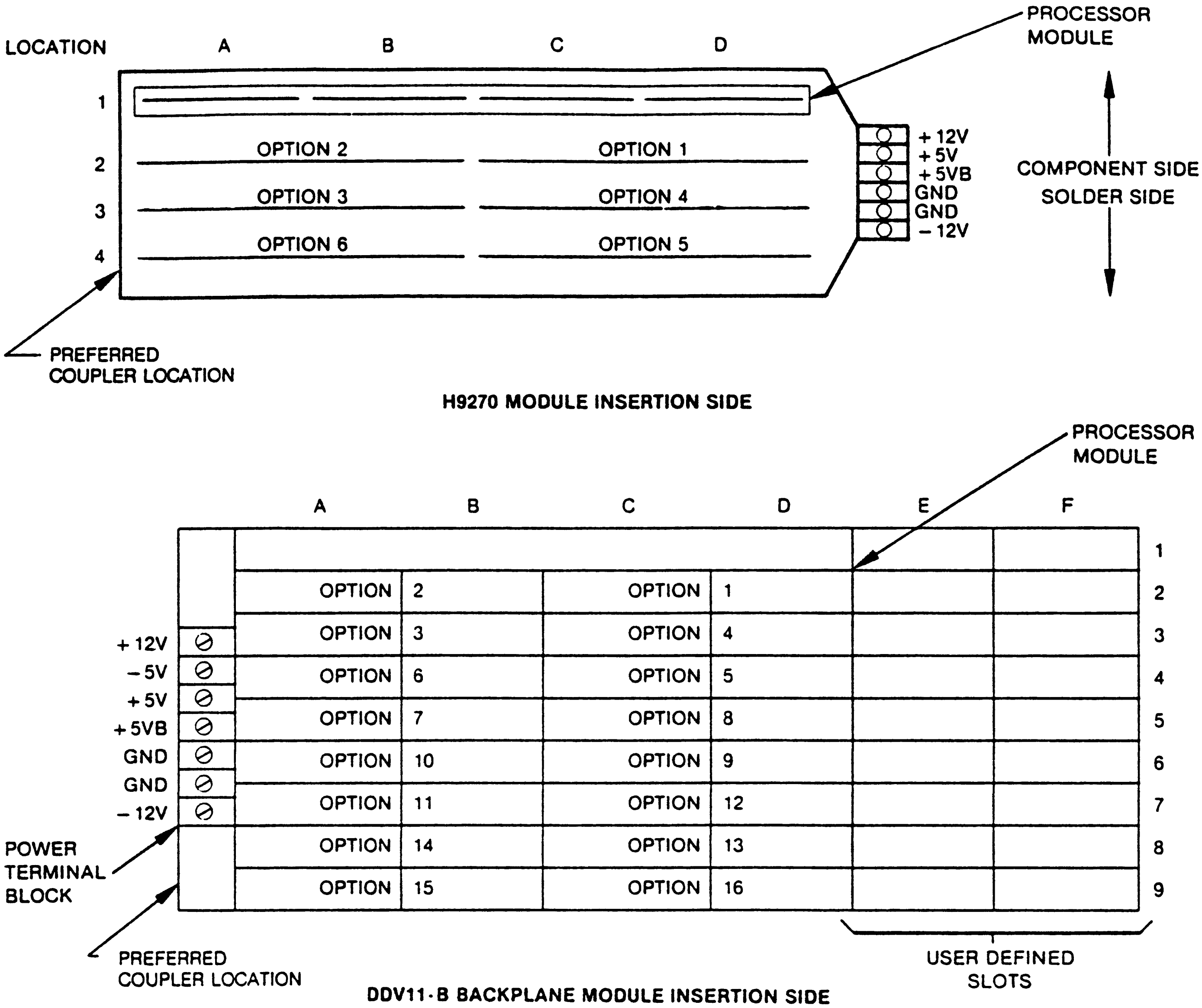
5. Refer to the mag tape manual for operating instructions and apply power to the drive and computer.

6. Observe that the green diagnostic LED on the controller board is lit.

7. The system is now ready to operate. Refer to Section 3 for operating instructions.

CONFIGURING THE COUPLER

The coupler board contains five groups of jumper locations, two board-edge mounted switches and a 10-switch switch pac that permit the user to configure a magnetic tape subsystem to meet specific requirements. Those configuration parameters that change infrequently are modified by jumpers; more frequently modified parameters are selected by switches. The coupler is shipped with jumpers installed and switches set to the "default" configuration, the configuration which is most commonly required.



NOTE

MEMORY CAN BE INSTALLED IN ANY SLOT; IT IS NOT PRIORITY DEPENDENT AND DOES NOT NEED TO BE ADJACENT TO THE PROCESSOR.

CONTROLLERS ARE ALSO COMPATIBLE WITH H9273A MODULES.

Figure 2-2. Typical Backplane Configuration

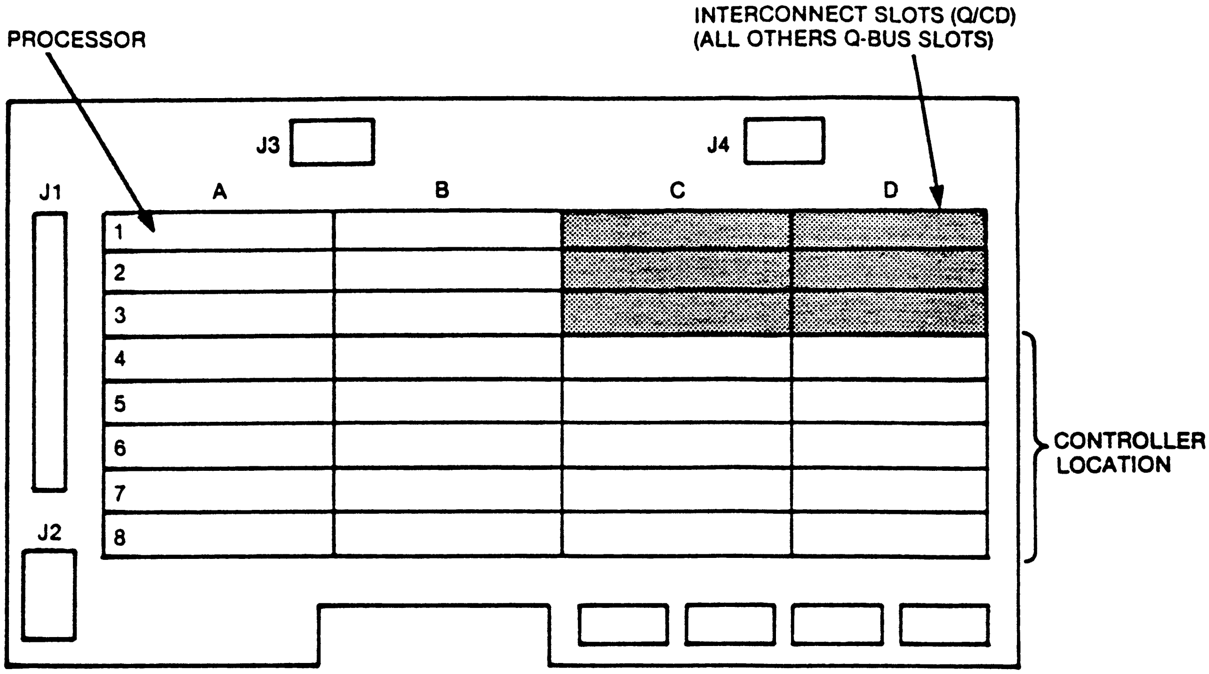
Figure 2-1 illustrates the locations of the jumpers and switches. Since the jumper positions are infrequently changed, the default configuration jumpers are etched on the PC board. Thus, to change jumpers, the board etch must be cut and jumpers added. The purpose of each jumper group and of the switches is as follows:

Controller Address Select Jumper

Jumper positions JP1, JP2, permit the register addresses of the controller to be changed. This feature is useful if the computer system already has one TS11 compatible tape system installed. Table 2-1 illustrates the jumper-position possibilities and resultant register addresses. Default settings are TSDB/TSBA=772 520 and TSSR=772 522 for logical unit zero.

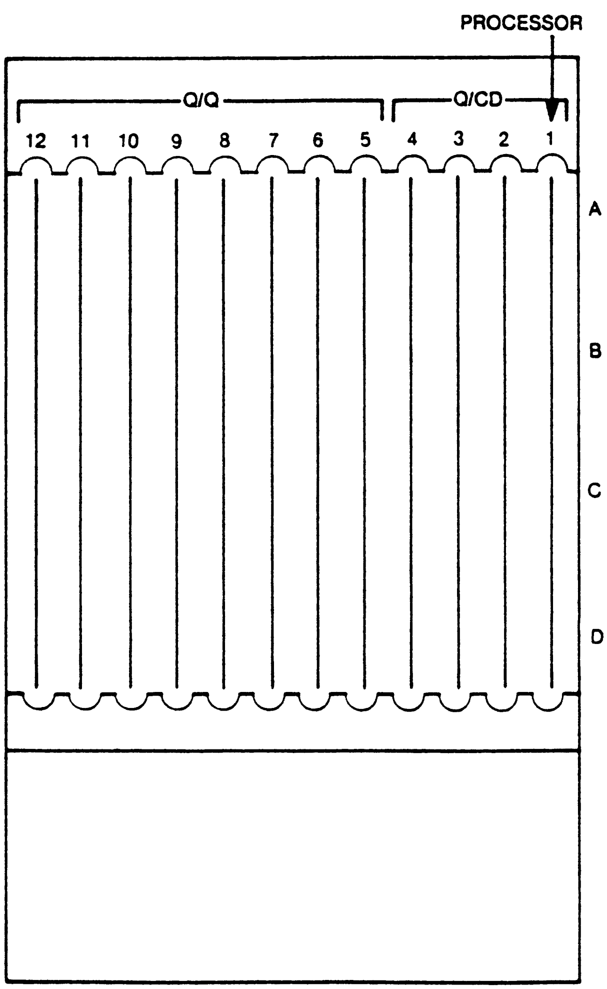
Interrupt Priority Level Select Jumpers

Jumper positions JP3, JP4, JP5 permit the interrupt priority level to be changed. Table 2-2 illustrates the jumper-position possibilities and resultant priority levels selected. Default setting is BR4.



NOTE: COMPONENTS ON THE BOARD MUST BE FACING TOWARDS THE PROCESSOR.

Figure 2-2A. MicroVAX II H9278 Backplane



NOTE: COMPONENTS ON THE BOARD MUST BE FACING TOWARDS THE PROCESSOR.

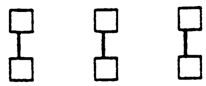
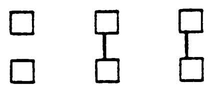
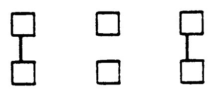
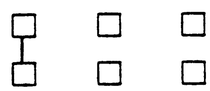
Figure 2-2B. MicroVAX II Backplane (Typical)

Table 2-1. Controller Address Select

Register Addresses TSDB/TSBA	Register Addresses TSSR	Logical Unit #	Jumpers Installed JP2	Jumpers Installed JP1	Jumper Configuration
772520	772522	0	Yes (Default)	Yes	JP1 JP2
772524	772526	1			
772530	772532	2			
772534	772536	3			
772720	772722	0	Yes	No	JP1 JP2
772724	772726	1			
772730	772732	2			
772734	772736	3			
777360	777362	0	No	Yes	JP1 JP2
777364	777366	1			
777370	777372	2			
777374	777376	3			
777420	777422	0	No	No	JP1 JP2
777424	777426	1			
777430	777432	2			
777434	777436	3			

Instructions for changing addresses: Remove any existing jumpers (including the one etched on the front of the board for the default setting) and install jumper shown for desired address. Diagram refers to the component side of the board.

Table 2-2. Interrupt Priority Level Selection

Jumper Configuration	Interrupt Priority Level
JP3 JP4 JP5 	Note: RSTS requires level 4. LEVEL 4 (Default)
JP3 JP4 JP5 	LEVEL 5
JP3 JP4 JP5 	LEVEL 6
JP3 JP4 JP5 	LEVEL 7
Instructions for changing interrupt priority level: Remove any existing jumpers (including those etched on the front of the board for the default setting) and install jumpers for the desired priority level as shown. Diagram refers to the component side of the board.	

Tape Drive Density and Speed Selection

Selection of tape drive density and speed is done manually at the tape drive.

Interrupt Vector, Extended Features, Drive Quantity Select Switches

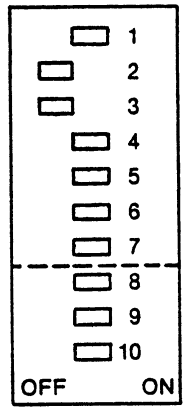
Switch SW2-2 selects the interrupt vector address for logical unit 0. The switch pac in board location 18B contains 10 two-position switches. Switches S1 through S7 select the starting address of a floating interrupt vector table for logical units 1, 2, and 3. Switch S8 enables Extended Features (18/22-bit addressing). Switches S9 and S10 define the number of logical units connected to the coupler. Table 2-3 shows the purpose of each switch position.

Interrupt Vector Address

If only one logical unit is connected to the coupler, switches S1 through S7 need not be set to any specific value, as switch S2-2 sets the interrupt vector address for logical unit zero. Switch 2-2 OFF selects address 224_8. Switch 2-2 ON selects address 274_8. If the coupler connects with more than one logical unit, then switches S1-S7 must be set to one of the floating interrupt vector addresses.

Table 2-3. Interrupt Vector, No. of Tape Drives, Extended Features (18/22-Bit Addressing), Long Gap Mode

LOCATION 18B
(Standard switch settings are shown)



ON = 0
OFF = 1

Logical Unit #	Interrupt Vector
0	Switch SW2-2 Selectable Factory set at 224 (SW2-2 OFF) SW2-2 ON = 274
1	SW1 Switches (Floating)
2	SW1 Switches + #4 (Floating)
3	SW1 Switches + #8 (Floating)

18/22-Bit Addressing	Disabled	Enabled
Switch SW1 #8	ON	OFF
Address Range	18 Bit	22 Bit

INTERRUPT VECTOR							
Switch SW1 #	1	2	3	4	5	6	7
Bit Position	8	7	6	5	4	3	2
Standard*	ON	OFF	OFF	ON	ON	ON	ON
(Octal)		3			0		0
*Standard switch settings show start of floating vectors.							

#Logical Units	1 (Std)	2	3	4
Switch SW1 #9	ON	ON	OFF	OFF
Switch SW1 #10	ON	OFF	ON	OFF

Long Gap Mode	Disabled	Enabled
Switch SW2-1	OFF	ON

The preferred vector address of the second unit is reflected in the switches. If the third and fourth units are enabled, their vector addresses are displaced four and eight addresses respectively above the address of the second drive. For example, if floating vector address 300_8 was assigned to the second drive, the vector address of drive three would be 304_8 and for drive four it would be 310_8. Default switch settings are 300_8.

Number of Logical Units

Switches S9 and S10 must be set to define the number of logical units connected to the coupler. Default values are S9 and S10 ON (one drive connected).

Extended Features

Switch S8 selects between 18- and 22-bit addressing and enables TSV05 compatibility. Only the TSV05 software handler supports 22-bit addressing on the Q Bus. The TS11/TU80 handler may require modifications to support 22-bit addressing on the Q Bus. Default value is S9 ON, selecting 18-bit main memory addressing.

Streaming Drive Long Gap Select Switch

Switch SW2-1 allows the operator to select "long gap" mode for PE or GCR streaming drives equipped with this option. The default switch setting is OFF. SW2-1 ON selects the long gap mode.

Note

DEC always *selects the long gap mode for their TU80 streaming tape subsystem. This 1600 cpi PE streamer operates at 100 ips in the high speed mode. The long gap mode can reduce the amount of data written on tape, depending on record size, software instruction times, tape drive Long Gap option type (fixed gap, variable gap), etc. Tapes with either normal or long gaps can be read regardless of the setting of SW2-1.*

The long gap mode should be selected when using any DEC disc backup software with a steaming tape drive. Selecting long gap mode does not mean that all inter-record gaps (IRG) written on tape will be long; for variable gap mode only, the gap length is primarily a function of software instruction times. Tapes with either normal or long gaps can be read regardless of the setting of SW2-1. Note that start/stop or cached tape drives do not have this option, thus, the SW2-1 switch setting is ignored.

The long gap mode merely extends the "reinstruct time" window of the streamer after the end of each record. This delays triggering the repositioning cycle longer than normal. Note that if the software does not provide sequential write instructions within the streamer reinstruct time, the streamer will enter a repositioning cycle which can take over one second. Table 2-4 compares normal and long gap reinstruct times for various models of PE and GCR tape drives.

If sequential software write commands occur within the normal reinstruct time window, a normal IRG will be erased. If sequential software write commands occur after the normal reinstruct time, but before the end of the long gap window, a longer IRG will be written but the drive will not enter the reposition cycle. If a sequential write command does not occur until after the long gap window time out, the repositioning cycle time penalty is invoked before a new write command can be accepted.

Therefore, the long gap mode is appropriate for two cases:

A. When streaming disc backup software usually generates the next write instruction within the normal reinstruct time window, but occasionally is delayed due to missing a disc rotation (seek command). This results in negligible loss of tape capacity because only a small percentage of tape records are followed by a longer than normal IRG.

B. When minimum time to perform a disc backup is more important than tape capacity, and the software usually cannot meet the

Table 2-4. Normal/Long Gap Reinstruct Time Comparisions

DRIVE	SPEED IPS	FORMAT	PE GAP (ms)				GCR GAP (ms)			
			NORMAL		LONG		NORMAL		LONG	
			WR	RD	WR	RD	WR	RD	WR	RD
Cipher F880	100	PE	3	4	7	8				
CDC 92181	100	PE	3.5	12	9.5	12				
CDC 92185	75	PE/GCR	5.5	15.5	13.5	15.5	1.5	3	5.5	7.5
DEC TU80	100	PE			9.5	12				
FUJ. M2442A	100	PE/GCR	4	5.5	10	11.5	1	2.5	4	5.5
STC 2922	100	PE/GCR	3.5	5	9.5	11	0.5	2	6.5	8

normal reinstruct time window requirements, but does fall within the long gap reinstruct time requirements. Even though longer than normal gaps are erased between records (reducing tape capacity), a high-speed streaming mode will be maintained to guarantee disc backup. If large record sizes are written to tape, the ratio of record size to blank tape will be such that good tape capacity may still be realized.

There is a major difference in reinstruct time between GCR and PE streaming tape drives even when operated at the same tape speed (see Table 2-4). This is because of the difference in the IRG size between the two formats: PE IRG size is 0.6 inch; GCR IRG size is 0.3 inch. Typical reinstruct times (normal gap) for 100 ips streamers in the write mode are 3.5 milliseconds in PE and 0.5 to 1.0 millisecond in GCR. Read mode reinstruct times are slightly longer because the physical distance between the write/read heads does not have to be subtracted from the gap spacing as is required for write mode calculations. This is because read-after-write parity checking is required in the write mode.

Since all DEC streaming software is designed for the TU80, PE streaming tape drive, which always has long gap mode selected, the long gap mode is recommended for both PE and GCR streamers when using DEC software. To re-emphasize, streaming performance is dependent upon software response time between records—not hardware response time.

Alternate Interrupt Vector Switch SW2-2

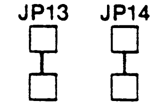
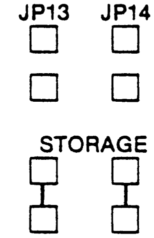
Switch SW2-2 allows the operator to select an alternate interrupt vector for logical tape unit zero. SW2-2 ON selects interrupt address vector 274 (octal). The default switch position is OFF, which selects standard interrupt address vector 224 (octal).

Coupler Jumpers for MicroVAX Backplane CD Slots

The DQ142 can be used with a MicroVAX computer with either a customer-supplied or DILOG-supplied driver for operation under MicroVMS. An additional group of jumpers has been added to the DQ142 to permit plugging the coupler into any slot of the MicroVAX backplane. All slots of the MicroVAX backplane are not wired the same. The A and B rows of the backplane conform with Q-bus wiring; most of the C and D rows also conform with Q-bus wiring. However, the first few slots (typically slots one through three or four) have the C and D rows interconnected to provide a private memory interconnect. These slots are wired differently than the Q-bus and are identified as the Q/CD bus.

Jumper positions JP13, JP14, JP15, JP16, JP17, and JP18 permit the coupler to be installed in any row of a MicroVAX backplane. Table 2-5 illustrates the jumper-position possibilities. Jumper positions JP13 and JP14 are configured with jumper plugs. Therefore, adjacent to these jumper locations are storage locations for these jumper plugs. This allows the coupler to be moved easily between computer slots, or between computers, for testing until a permanent slot location is selected. Note that JP13 and JP14 perform the function of an M9047 grant continuity card in standard Q-bus CD rows. Jumpers JP15, JP16, JP17, and JP18 pick up additional ground connections for the coupler from the D row. While moving the coupler among rows or computers for testing, it is not critical that these jumpers be installed. However, if a permanent location in slots four through eight is selected for installation, these jumpers can be installed (soldered wire) to provide added noise rejection for signals on the coupler.

Table 2-5. Coupler Jumpers for MicroVAX Backplane

Jumper Configuration	Coupler Backplane Slot Location
JP13 JP14 	Q/Q Slots (Default)
JP13 JP14 STORAGE 	Q/CD Slots

Storage is provided for the jumper plugs used for JP13 and JP14. Diagram is for component side of the board.

SECTION 3
OPERATION

INTRODUCTION

Prior to operating the system, the instruction manual sections describing the controls and indicators on the tape drive and procedures for mounting and removing tape reels should be read. To prevent loss of data or damage to the magnetic tape, the following precautions should be observed:

a. Always handle a tape reel by the hub hole. Squeezing the reel flanges can cause damage to the tape edges when winding or unwinding tape.

b. Never touch the portion of tape between the BOT and EOT markers. Oils from fingers attract dust and dirt. Do not allow the end of the tape to drag on the floor.

c. Never use a contaminated reel of tape. This spreads dirt to clean tape reels and can affect tape drive operation.

d. Always store tape reels inside their containers. Keep empty containers closed so dust and dirt cannot get inside.

e. Inspect tapes, reels, and containers for dust and dirt. Replace take-up reels that are old or damaged.

f. Do not smoke near the tape drive or tape storage area. Tobacco smoke and ash are especially damaging to tape.

g. Do not place the tape drive near a line printer or other device that produces paper dust.

h. Clean the tape path frequently.

Note that tape drives permit off-line or on-line operation. The off-line mode is controlled by switches on the tape drive. The on-line mode is controlled by programmed commands from the computer via the coupler and formatter. When system operation is desired, be sure the tape drive ON-LINE indicator is lit. On-line operation is a function of program commands described in Section 4 of this manual.

Tape Format

For detailed information on tape format characteristics see formatter and tape drive manuals.

Booting From Magnetic Tapes

1. Place the tape transport "ON LINE" and position the tape at "Beginning of Tape."
2. If the CPU is equipped with a TS11 hardware bootstrap, simply type "MS0" <CR> (RETURN key). If no hardware bootstrap is installed, boot is shown in Table 3-1 or Table 3-2. Table 3-1 is an abbreviated boostrap routine.

Table 3-1. TSV05 Short Bootstrap Routine

Address	Data	Code
001000	012701	MOV #TSSR, R1
001002	172522	
001004	012704	MOV #NUM + 20, R4
001006	001046	
001010	112737	MOV B200, 172523
001012	000200	
001014	172523	
001016	105711	TSTB (R1)
001020	100376	BPL. – 2
001022	005000	CLR R0
001024	005007	CLR PC
001026	046523	NUM = MS (ASCII)

DIAGNOSTICS

On-line and off-line diagnostics and switch settings for the tape drive are described in the tape drive manual. The green diagnostic LED on the coupler board indicates the coupler passed self test when lit.

The DEC software diagnostics and "exerciser" programs that can be run with the coupler depend upon the computer and software operating system being used.

Note

Some of the functional tests report invalid errors when cached tape drives are used with the coupler. These errors occur in subtests that involve specific time delay measurements and simulate detection of blank tape. For example, after erasing a long gap

Table 3-2. TS11 / TU80 / TSV05 Bootstrap Routine

Address	Data		Code			
			TSBA	=	172520	TS11 ADDRESS REGISTER ADDRESS
			TSSR	=	172522	TS11 STATUS REGISTER ADDRESS
001000	012700	172520	START:	MOV	#TSBA, R0	GET ADDRESS OF TSBA INTO R0
001004	012701	172522		MOV	#TSSR, R1	GET ADDRESS OF TSSR INTO R1
001010	005011			CLR	(R1)	INIT AND REWIND TAPE
001012	105711			TSTB	(R1)	TEST IF 'SSR' IS SET
001014	100376			BPL	. − 2	AND WAIT UNTIL IT IS
001016	012710	001064'		MOV	#PKT1, (R0)	ISSUE SET-CHARACTERISTICS COMMAND
001022	105711			TSTB	(R1)	TEST IF 'SSR' IS SET
001024	100376			BPL	. − 2	AND WAIT UNTIL IT IS
001026	012710	001104'		MOV	#PKT2, (R0)	SKIP OF FIRST RECORD (HEADER FILE)
001032	105711			TSTB	(R1)	TEST IF 'SSR' IS SET
001034	100376			BPL	. − 2	AND WAIT UNTIL IT IS
001036	012710	001104'		MOV	#PKT2, (R0)	ISSUE READ OF SECOND RECORD (MS)
001042	105711			TSTB	(R1)	TEST IF 'SSR' IS SET
001044	100376			BPL	. − 2	AND WAIT UNTIL IT IS
001046	005711			TST	(R1)	ANY ERRORS ? ? ? ?
001050	100421			BMI	HLT	HALT IN FRONT OF MESSAGE IF ERRORS
001052	012704	001102'		MOV	#NUM + 20,R4	ADDRESS OF 'NUM' + 20 TO REG. 4
001056	005000			CLR	R0	0 ·R0 (UNIT #0)
001060	005007			CLR	PC	RESUME EXECUTION AT ZERO IF NO ERRORS
001062	046523		NUM:	046423_8		MS (ASCII)
				SET-CHARACTERISTICS PACKET		
001064	140004		PKT1:	140004		COMMAND (SET CHARACTERISTICS)
001066	001074'			PK		LS ADDRESS OF PACKET
001070	000000			0		MS ADDRESS OF PACKET
001072	000010			8.		NUMBER OF BYTES IN PACKET
001074	001116'		PK:	MES		LS ADDRESS OF MESSAGE PACKET (END STATUS)
001076	000000			0		MS ADDRESS OF MESSAGE PACKET
001100	000016			14.		NUMBER OF BYTES IN PACKET
001102	000000			0		
				READ-DATA PACKET		
001104	140001		PKT2:	140001		COMMAND (READ ONE RECORD)
001106	000000			0		LS BUFFER START ADDRESS
001110	000000			0		MS BUFFER START ADDRESS
001112	001000			512.		NUMBER OF BYTES
001114	000000		HLT:	HALT		
001116			MES:			START OF 7 WORD MESSAGE PACKET (END STATUS)

on tape, an OPI error is expected when the tape is re-read. The OPI error will not be generated when testing a cached tape subsystem. The known error caused by cached tape subsystems are noted where appropriate in the following text.

VAX:

A. EVMAA TS11 Data Reliability (see note 1)
B. EVMBD TU80 Functional Test #1
C. EVMBE TU80 Functional Test #2

PDP-11 XXDP+:

A. CZTUVB0 TU80 Data Reliability
B. CZTUWA0 TU80 (no drive)
C. CZTUXA0 TU80 Functional Test #1 (see note 2)
D. CZTUYA0 TU80 Functional Test #2 (see note 3)
E. CZTUZA0 TU80 Functional Test #3 (see note 4)
F. CZTSHC0 TS11 Data Reliability
G. CXTSAA0 TS11 DEC/X11 System Exerciser

OPERATING SYSTEM SOFTWARE

Most DEC operating system software packages include some form of concurrent DMA I/O exerciser tests. In some cases these tests can be run even while the operating system is on line—as long as the peripherals to be tested are either not in use or, like discs, can have a reserved area assigned.

These exercisers are typically called UETP (User Environment Test Package), IOX (Input/Output Exerciser), or MTEXER (Magnetic Tape Exerciser).

The best way to run these exerciser tests is to activate testing on more than one DMA device simultaneously (such as disc and magnetic tape). In this way concurrent DMA operations are also tested.

NOTES:

1. Reports two "Data Compare Errors" when run on the VAX11/780. However, this is normal even for the DEC TS11. If EVMAA is run in the on-line mode, no errors should be reported.

2. CZTUXA0 diagnostic test 4 verifies that the coupler returns Non Existent Memory (NXM) status for DMA memory transfer attempts into the upper 8K byte I/O page.

   Two invalid error messages occur if during DMA transfers computer memory increments across the upper 8K byte I/O page memory boundary or the coupler subsystem contains a cache tape that has a limit on the maximum record size.

   The first error typically occurs when more than 248K bytes of memory is installed. If the following error occurs, check the memory configuration options:

   A. Error 418, test 4, subtest 4, PC 037254 Error Message, "TSSR not correct after WRITE command reject due to NXM."

   The second error is due to the cache tape drive's limitation on maximum record size. The cache tape can be internally configured to define the maximum record size. Typical configurations are between 16K and 24K bytes. The diagnostic causes the coupler to advance through DMA memory addresses until either addresses past installed memory are issued or addresses are issued into the I/O page. This should cause NXM status to be reported by the coupler. The diagnostic does this by writing several large records (approximately 62K bytes), which causes the coupler to advance through computer memory until available memory is exceeded and NXM is generated. Unfortunately, the cache tape goes into a "drive fault" mode if the configured maximum record size is exceeded. This results in the following error:

   A. Error 421, test 4, subtest 5, PC 037520 Error Message, "TSSR not correct after WRITE to non-existant memory."

   The following software patch will cause this diagnostic test to operate correctly with a cache tape:

   A. Address=37412: was=0, patch to=1

3. Test 3, subtest 5 reports invalid error 355 at PC 055434 if cache tape is used with the coupler. The error message is, "write data retries erase tape not long enough."

4. Test 4, subtest 3 reports invalid errors 427/428 at PC 050772, 051026, 050772 if cache tape is used with the coupler. The error messages are as follows:

   A. Erase failed to clear (ERASE) tape properly.

   B. OPI bit (XST3) failed to set.

   Test 5, subtest 1 reports invalid errors 517/526 at PC 054200, 055014 if cache tape is used with the coupler. The error message is, "unable to clear EOT indication, bit 0 (XST0)."

SECTION 4
PROGRAMMING

PROGRAMMING DEFINITIONS

FUNCTION: The expected activity of the tape system (read, write, rewind).

COMMAND: The instruction which initiates a function.

INSTRUCTION: One or more orders executed in a prescribed sequence that cause a function to be performed.

ADDRESS: The binary code placed on the A00L-A17L lines by the bus master to select a register in a slave device. Note that "register" can be either discrete elements (flip-flops) or memory elements (core, solid state RAM or ROM). When addressing devices other than computer internal memory, i.e., peripheral device registers, the upper 4K words address space is used.

REGISTER: An associated group of memory elements that react to a single address and store information (status, control, data) for use by other assemblies of the total computer system.

PROGRAM SEQUENCES

Commands, data, and status are sent between the coupler and the processor (CPU) in groups of bytes called "packets." There are four types of packets:

1. Command packet
2. Data packet
3. Characteristics packet
4. Message packet (also called end packet). A summary is shown at the end of this section.

The packets are established in main memory by the CPU. Typically there are two main memory packet (buffer) areas: Data buffers and control/status buffers. Both areas can be controlled by either the CPU or the coupler. The buffer contents and sources are as follows:

Data Buffer	Packet Buffer	Size	Source
	command	8 bytes	CPU
data from tape		1 byte to 65 Kbytes	Coupler
data to tape		1 byte to 65 Kbytes	CPU
	set characteristics	6-10 bytes	CPU
	message	14-16 bytes	Coupler

This packet technique for communicating between the CPU and the coupler improves computer system efficiency by reducing the number of information transfers to and from the tape system under processor control; in addition to data transfers, status and command information is transferred via the DMA facility.

The coupler has two program-accessible registers: the status register (TSSR) and the combination data buffer/bus address register (TSDB/TSBA). Additional status reflecting the state of the tape subsystem is stored in the message packet buffer located in main memory.

A typical read or write command sequence is as follows:

1. CPU reads status register (TSSR).
2. CPU loads (writes) data buffer register (TSDB) with starting address of a command packet, which is then shifted and loaded into the internal TSBA register of the coupler.
3. The controller accesses the command packet, which is typically "set characteristics." Note that the set characteristics command packet comprises 3 to 5 successive memory locations (6-10 bytes) that contain (see Figure 4-1):

   A. Command header word

   B. Least significant bits of characteristic packet address

   C. Most significant bits of characteristic packet address

   D. Byte count of characteristics packet

   The contents of the set characteristics packet are now accessed by the coupler. The principle purpose of executing this command is to get the starting address of the end message packet. Upon conclusion of a read or write operation, the message packet locations are loaded with status words by the coupler.
4. CPU loads Data Buffer Register (TSDB) with starting address of the next command packet, which is then shifted and loaded into the TSBA register of the coupler.

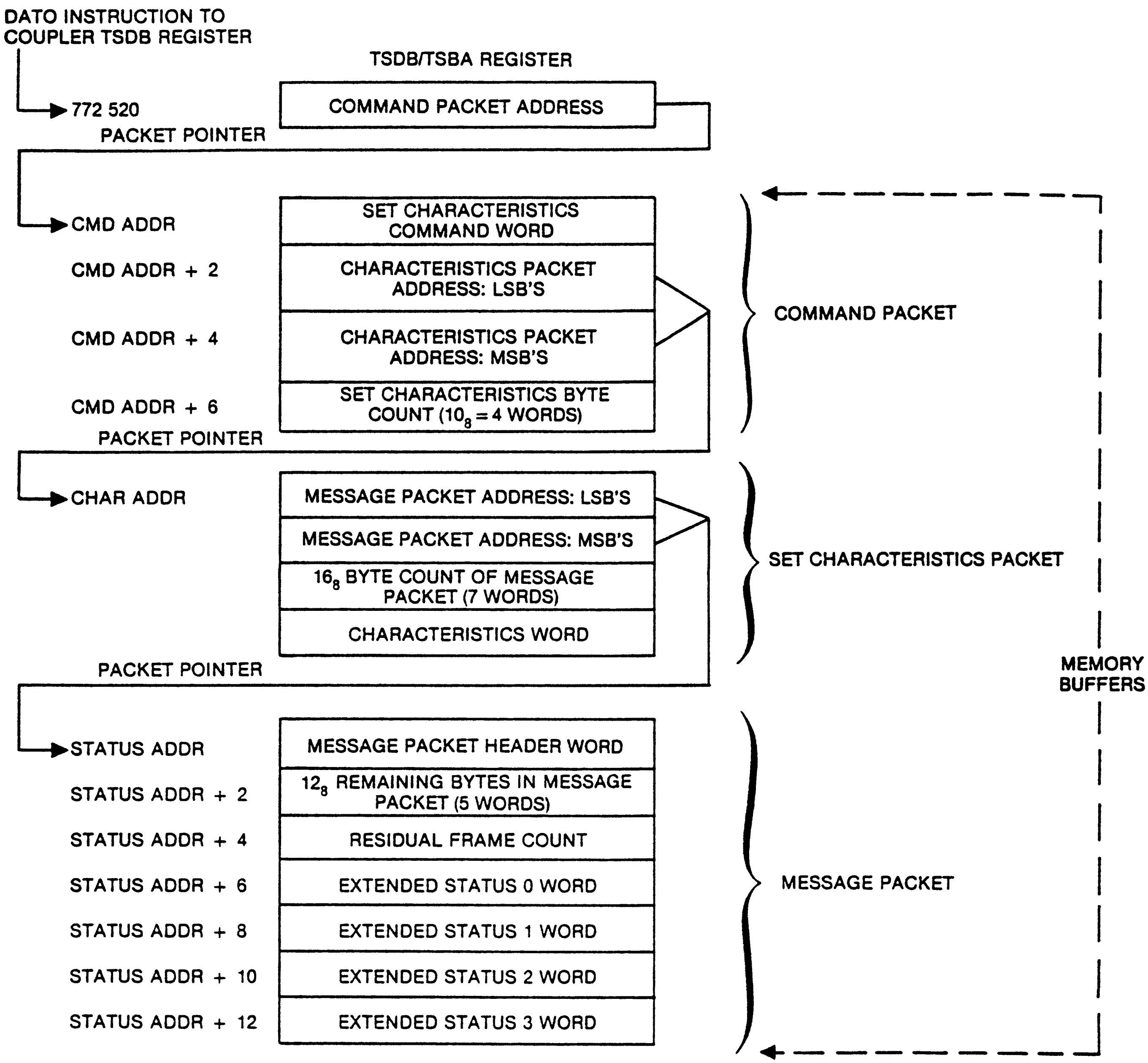


Figure 4-1. Typical SET CHARACTERISTICS Command Sequence

5. The coupler TSBA contents access the next command packet. Read/write command packets comprise four successive memory locations (eight bytes) that contain (see Figure 4-2):

   A. Command header word.

   B. Least significant bits of starting location in memory, where data is to be read from (write command) or written to (read command).

   C. Most significant byte of starting memory location.

   D. Number of bytes to be transferred (byte count).

6. The coupler as bus master now begins the transfer of data between main memory and the selected tape drive.

7. Reading or writing of data continues until either the proper byte count is reached or until the end of a record (reading) is detected.

8. Status information is now loaded into:

   A. Register TSSR in the coupler

   B. The message packet as defined by the last set characteristics command.

9. If instructed, the coupler generates an interrupt to signal the end of a command.

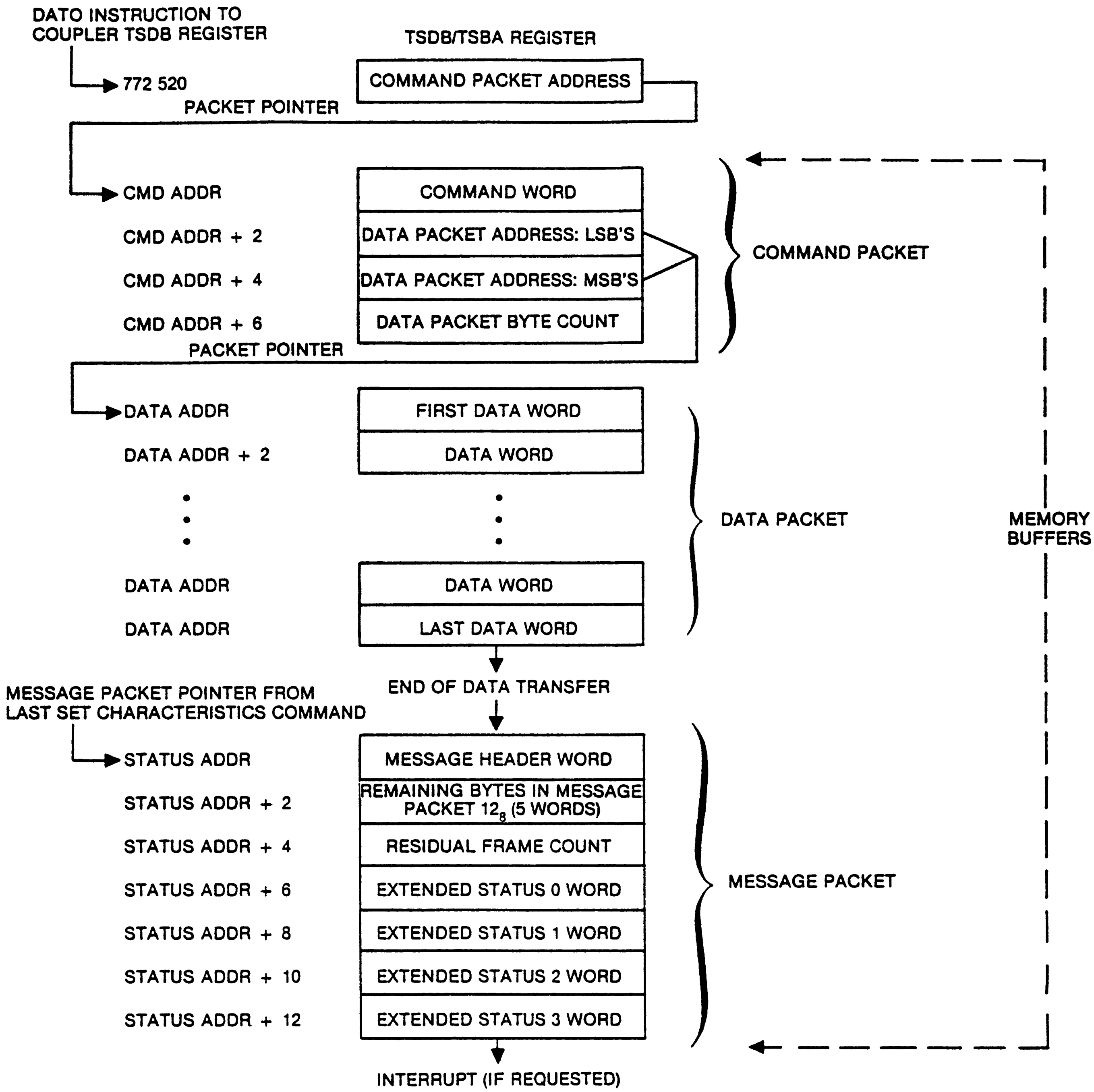


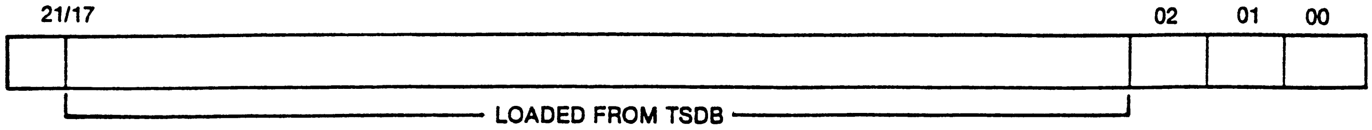
Figure 4-2. READ/WRITE Command Sequence

A "set characteristics" command packet was mentioned in step 3 of the read/write command sequence. The purpose of this command is to load the starting address of the message packet into the coupler, and to load a characteristics word into the coupler. The characteristics word defines certain options that are available to the software.

REGISTERS AND PACKETS

The following material describes the coupler registers and illustrates and describes the contents of the packets.

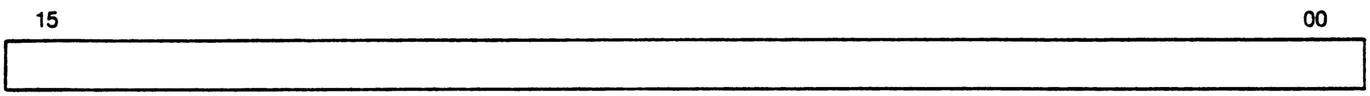
BUS ADDRESS REGISTER (TSBA) Read Only—Same Address as TSDB
772 520 (Transport 0) **772 530 (Transport 2)**
772 524 (Transport 1) **772 534 (Transport 3)**



The lower 18 bits of this 18/22-bit register are parallel loaded from the TSDB each time the TSDB is loaded as a slave by the CPU. TSDB bits 15-2 load into TSBA bits 15-2; TSDB bits 1 and 0 load into TSBA bits 17 and 16. Zeros are loaded into TSBA bits 1 and 0, specifying a Modulo-4 address. TSBA bits 17-16 are displayed in status register (TSSR) bits 9 and 8 respectively. TSBA is a read-only register that contains the address of the last word read from or written into memory.

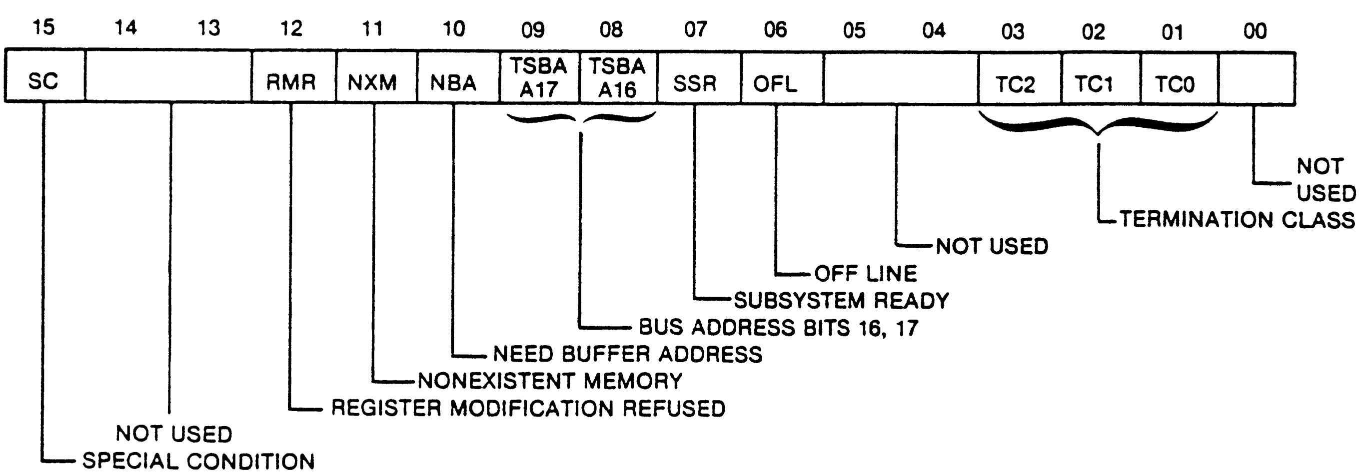
The 22-bit version of this register is only supported by the TSV05 handler, and is enabled by the EXTENDED FEATURES switch. TSBA bits 18-21 are loaded via a write to the TSDBX register and are not displayed (cannot be read).

DATA BUFFER REGISTER (TSDB) Write Only—Same Address as TSBA
772 520 (Transport 0) **772 530 (Transport 2)**
772 524 (Transport 1) **772 534 (Transport 3)**



This 16-bit register is parallel loaded from the Q Bus. This register, when loaded, provides the coupler with the memory location of a command packet. The command packet pointer is shifted and copied into 16-bits of the TSBA to form the command packet address. When the controller is bus slave, the TSDB can be loaded by three different transfers from a bus master; two transfers are for maintenance purposes (DATOB to high byte and DATOB to low byte); the third transfer is for normal command initiation (DATO). This register is write-only and is not cleared by subsystem initialize, or bus initialize. The coupler responds with BRPLY any time the TSDB is written.

STATUS REGISTER (TSSR) Read/Write (Write causes initialize and rewind to BOT)
772 522 (Transport 0) **772 532 (Transport 2)**
772 526 (Transport 1) **772 536 (Transport 3)**



In addition to this register, the coupler provides additional information in the Message Packets that it loads into main memory at the termination of each command.

Status Register Bit Definitions

Bit	Name	Termination Class (TC) Octal Code	Definition
00	—	—	Not Used.
01	TC0	—	Termination Class Bit 00: See TC2 (bit 03) below.
02	TC1	—	Termination Class Bit 01: See TC2 (bit 03) below.
03	TC2	—	Termination Class Bit 02: This bit, along with the TC1 and TC0 bits, acts as an offset value when an error or exception condition occurs on a command. Each of the eight possible values of this field represents a particular class of errors or exceptions. The code provided in this field is expected to be utilized as an offset into a dispatch table for handling the condition. These bits are useful only when special condition (SC) bit 15 is set. See Table 4-1.
06	OFL	—	Off-Line: When set, this bit indicates that the transport is off-line and unavailable for any tape motion commands.
07	SSR	—	Subsystem Ready: When set, this bit indicates that the subsystem is not busy and is ready to accept a new command pointer.
08	A16	—	Bus Address Bit 16: See A17 below (bit 09).
09	A17	—	Bus Address Bit 17: A17 and A16 (bits 08 and 09) display the values of bits 17 and 16 in the TSBA register.
10	NBA	—	Need Buffer Address: When set, this bit indicates that the transport needs a message buffer address. This bit is cleared after successful completion of a Set Characteristics command; it is always set after subsystem initialization.
11	NXM	4/5	Nonexistent Memory: This bit is set by the controller when trying to transfer to or from a memory location which does not exist. It may occur when fetching the command packet, fetching or storing data, or storing the message packet.
12	RMR	—	Register Modifications Refused: This bit is set by the controller when a command pointer is loaded into TSDB and Subsystem Ready (SSR) is not set. This bit may set a bug-free system if ATTN interrupts are enabled.
13	—	—	Not Used.
14	—	—	Not Used.
15	SC	—	Special Conditions: When set, this bit indicates that the last command was not completed without incident. Specifically, either an error was detected or an exception condition occurred. An exception condition could be a tape mark on read commands, reverse motion at BOT, EOT while writing, etc.

Table 4-1. Status Register Termination Class Codes

TSSR Bits 3, 2, 1	Description
000	Normal termination.
001	Attention Condition: Set by change in offline (bit 06) or a microdiagnostic failure defined by Extended Status 3 word.
010	Tape Status Alert: Set by tape mark, short records, long records, or EOT bits in Extended Status 0 word.
011	Function Reject: Set by off line, write lock error, illegal command, illegal address, on-line status change, or BOT in Extended Status 0 word.
100	Recoverable error (tape position—one record down from start of function)
101	Recoverable error (tape not moved)
110	Unrecoverable error (tape position lost)

EXTENDED DATA BUFFER REGISTER (TSDBX)—TSV05 Only

772 523 (Transport 0)
772 527 (Transport 1)
772 533 (Transport 2)
772 537 (Transport 3)

LSI-11 Bus Bits:	15	14	13	12	11	10	09	08
High Byte Data Bits:	07	06	05	04	03	02	01	00
	BT	0	0	0	A21	A20	A19	A18

TSDBX is supported only by the TSV05 handler and is a write-only hardware byte register located at the fourth byte address of the I/O register block; this address corresponds to the high-order byte of the TSSR register. The TSDBX is used to specify the most significant four bits of a 22-bit command pointer address and to allow an automatic tape boot sequence to be performed.

TSDBX can be written only by a byte-access (DAT0B) cycle addressed to the high byte of TSSR. If the EXTENDED FEATURES switch is OFF when the TSDBX is written, only the Boot bit (07) is examined; the other bits are ignored.

If the EXTENDED FEATURES switch is ON when TSDBX is written, the contents of the least significant four bits of TSDBX are transferred to bits 18 through 21 of the internal TSBA (bus address) register for use as a command pointer. The low order 18 bits of the command pointer are specified by writing into the TSDB register, which starts an operation and then clears TSDBX. Therefore, a subsequent load of only the TSDB will specify a 22-bit command pointer address with the high-order four bits equal to zero.

For the TSDBX register to be properly written, the SSR (Subsystem Ready) bit in TSSR must be set; if it is not, the RMR (Register Modification Refused) bit will be set and no modification to TSDBX will occur. When the TSDBX is written, the SSR bit is not cleared. Therefore, RMR should be checked, before TSDB is written. Writing the TSDB will begin processing on TSDBX. If the Boot bit is *not* set, the command pointed to by the 22-bit TSDB will be retrieved and command processing will begin. If the Boot bit is set, SSR will remain clear until the boot sequence is complete or until an error occurs.

Extended Data Buffer Register (TSDBX) Bit Definitions

Bit	Name	Definition
00-03	A18-A21	Command Pointer bits 18-21. When the TSDBX is written, and SSR=1, the data is loaded into bits 18-21 of the internal TSBA register. TSDBX is cleared after TSDB is written and is also cleared by Initialize.
04-06	—	Reserved. Should always be written to 0.
07	BT	Boot Command Bit: When written to 1, with SSR=1, causes the tape to be rewound to BOT, the first tape record to be skipped, and the second record (only the first 512 bytes of it) to be loaded into CPU memory space starting at location 0.

COMMANDS

The functions listed in Table 4-2 make up the Tape Subsystem Command Set. Some commands have various subcommands, termed "modes." The device registers are used to initiate command packet processing and retrieve basic status.

Commands are not written to the coupler registers. Instead, command pointers, which point to a Command Packet somewhere in CPU memory, are written to the TSDB register. The Command Packet instructs the coupler about the function to be performed. These words contain function parameters such as bus address, byte count, record count, and modifier flags.

Before the coupler begins a function, the CPU must assemble the command packet in main memory. The command packet is always four words long, although not all commands use all four of the words in the packet. The words in the command packet may be thought of as the contents of several registers. The first word in a command packet is called the Header-word. Command types are detailed in the following paragraphs.

Table 4-2. Assigned Commands

Command Name	Mode Name/Description
GET STATUS	Get Status (update the message buffer in memory).
READ	Read Next (Forward) Read Previous (Reverse) Reread Previous (Space Reverse, Read Forward or Read Reverse, Space Forward) Reread Next (Space Forward, Read Reverse or Read Forward, Space Reverse)
WRITE CHARACTERISTICS	Load Message Buffer Address and Set Device Characteristics
WRITE	Write Data Write Data Retry (Space Reverse, Erase, Write Data)
POSITION	Space Records Forward Space Records Reverse Skip Tape Marks Forward Skip Tape Marks Reverse Rewind
FORMAT	Write Tape Mark Erase Write Tape Mark Retry (Space Reverse, Erase, Write Tape Mark)
CONTROL	Message Buffer Release Rewind and Unload Clean Tape (handled as a NO-OP) Rewind with Immediate Interrupt (TSV05 only)
INITIALIZE	Coupler/Drive Initialize

Command Packet: Command Word Data Buffer Address, Byte Count

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ACK	CVC	OPP	SWB	COMMAND MODE				FMT 1			HDS	COMMAND CODE			
A15 ← LOW-ORDER DATA BUFFER ADDRESS → A00															
0 ← ALL ZEROES → 0 HIGH ORDER DATA BUFFER ADDRESS										A21	A20	A19	A18	A17	A16
← DATA BUFFER EXTENT (BYTE COUNT) (16 BIT POSITIVE INTEGER) →															

Command Word Bit Definitions

Bit	Name	Definition
0-3	Command Code Field	Used with command mode field to specify tape subsystem commands. See bits 8-11 and Tables 4-3 and 4-4.
4	HDS	High density or streaming select = 1; low density or stop/start = 0.
5-7	Format 1	The following two values are defined in this field. If interrupt enable on, interrupt is generated when SC bit or ready bit (status register) sets. **Bit Values** — **Definition** 000 — Interrupt disable 100 — Interrupt enable
8-11	Command Mode Field	Used with command code field to specify tape subsystem commands. See Tables 4-3 and 4-4.
12-14	Device Dependent Bits	These three bits are implemented as follows: **Bit** — **Name Definition** 14 — CVC Clear volume check 13 — OPP opposite (reverse the execution sequence of the reread commands). 12 — SWB, Swap Bytes. SWB = 1 is the industry standard (beginning with an even byte). When SWB = 0, the swapping begins with an odd byte.
15	Acknowledge	This bit is set when a command is issued by the CPU. States that the message buffer is now available to the coupler for any pending or subsequent message packets. Passes control of the message buffer to the coupler.

Table 4-3. Command Code and Mode Field Definitions—Standard

Command Code Field	Command Name	Command Mode Field	Mode Name
00001	Read	0000	Read next (forward)
		0001	Read previous (reverse)
		0010	Reread previous (space reverse, read forward or read reverse, space forward)
		0011	Reread next (space forward, read reverse or read forward, space reverse)
00100	Set Characteristics	0000	Set status message packet address and device characteristics word.
00101	Write	0000	Write data
		0010	Write data retry (space reverse, erase, write data)
01000*	Position	0000*	Space records forward
		0001*	Space records reverse
		0010*	Skip tape marks forward (space files)
		0011*	Skip tape marks reverse (space files)
		0100**	Rewind
01001**	Format	0000	Write tape mark
		0001	Erase (erase 3 inches of tape)
		0010	Write tape mark retry (space reverse, erase, write tape mark)
01010**	Control	0000	Message packet release
		0001	Rewind and unload
		0010	Clean (handled as a NO-OP)
		0100	Rewind with immediate interrupt (TSV05 only)
01011**	Initialize	0000	Drive initialize
01111**	Get status	0000	Get status (End Message Packet)

*Two-word command packet
**One-word command packet

Table 4-4. Command Code and Mode Field Definitions—Streaming*

Command Code Field	Command Name	Command Mode Field	Mode Name
10001	Read Streaming	0000	Read next (forward)
		0001	Read previous (reverse)
		0010	Reread previous (space reverse, read forward)
		0011	Reread next (space forward, read reverse)
10101	Write Streaming	0000	Write data
		0010	Write data retry (space reverse, erase, write data)
11000**	Position Streaming	0000	Space records forward
		0001	Space records reverse
		0010	Skip tape marks forward (space files)
		0011	Skip tape marks reverse (space files)
		0100	Rewind
11001***	Format Streaming	0000	Write tape mark
		0001	Erase (erase 3 inches of tape)
		0010	Write tape mark retry (space reverse, erase, write tape mark)

*Jumper JP6 to FDEN, JP7 to FTAD0, and JP8 to FTAD1.
**Two-word command packet
***One-word command packet

TWO-WORD COMMAND PACKET: Command Word and Count

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ACK	CVC	0	0	COMMAND MODE				IE	FORMAT 0	0	COMMAND CODE				
← TAPE MARK/RECORD COUNT (16 BIT POSITIVE INTEGER) →															

This command causes the tape to space records forward or reverse, skip tape marks forward or reverse, or to rewind to BOT. An exact tape mark/record count must be the second word of the packet for Skip Tape Mark and Space Record commands.

A Space Records operation automatically terminates when a tape mark is traversed. Also, Record Length Short (RLS) is set if the record count was not decremented to zero.

A Skip Tape Marks command terminates when it encounters a double tape mark and the Enable Skip Stop mode is specified (ESS bit set) in the characteristics word. Termination will also occur if a tape mark is the first record off BOT and ESS and ENB bits are set in the characteristics word. Record Length Short (RLS) is set if the record count is not decremented to zero.

A Space Records Reverse or Skip Tape Marks Reverse, which runs into BOT, sets Reverse Into BOT (RIB) and causes a tape status alert termination.

Note

If the tape is positioned between BOT and the first record and a space reverse or skip reverse is done, RIB will set and the residual frame count will equal the specified count in the original command.

SET CHARACTERISTICS COMMAND

Table 4-5 illustrates the Set Characeristics Command and Data Packets. This command informs the coupler of the location and size of the message buffer in the CPU memory and also defines some specific controls required when executing other commands. If successfully completed, this command clears the Need Buffer Address (NBA) bit in TSSR. If the command is rejected because an illegal address was specified, NBA will be set.

The second and third words of the Set Characteristics command give the address of the characteristics data buffer. This buffer must reside on an even address boundary in CPU memory. If bit 0 of the second packet word (low order characteristics data buffer address) or bits 2-15 (extended features disabled) or bits 6-15 (extended features enabled) of the third packet word (high order characteristics data buffer address) are not zero, the command is rejected and no message packet is sent. However, if the IE bit is set in the command packet header word, an interrupt will be generated.

The fourth word of the Set Characteristics Command Packet specifies the number of bytes of the characteristics data buffer. Only values of decimal six, eight, or 10 (extended features enabled) are valid. If a byte count of less than 6 is specified, the command will be rejected. If too large a value is given, the default setting will be used; if extended features are disabled, default is decimal eight; if extended features are enabled, default is decimal 10. Note that only the TSV05 handler supports settings of 6 or 10 bytes. If extended features are disabled and the specified buffer size is six, then the characteristics mode data word portion of the characteristics data packet will not be fetched and the current value of the characteristics mode control bits will be retained. If extended features are enabled and the specified buffer size is either six or eight, the extended characteristics data word will not be fetched and the current values will be retained. If not specified, the characteristics mode data word and extended characteristics data word will default to zero.

Table 4-5. SET CHARACTERISTICS Command Format

SET CHARACTERISTICS Command Packet

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEVICE DEP.			MODE				FORMAT 1			COMMAND				
ACK	CVC	0	0	0	0	0	0	IE	0	0	0	0	1	0	0
A15	LOW ORDER SET CHARACTERISTIC DATA ADDRESS													A01	0
0	HIGH ORDER CHARACTERISTIC DATA ADDRESS								0	(TSV05 ONLY) A21			A18	A17	A16
BUFFER EXTENT (Byte Count) (16-Bit Positive Integer)															

Characteristics Data Packet

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
A15	LOW ORDER MESSAGE BUFFER ADDRESS													A01	0
0	HIGH ORDER MESSAGE BUFFER ADDRESS								0	(TSV05 ONLY) A21			A18	A17	A16
LENGTH OF MESSAGE BUFFER (At Least 14 bytes long) (16-Bit Positive Integer)															
0	RESERVED						0	ESS	ENB	EAI	ERI	RESERVED 0	0	0	0
NOT USED										HDS	NOT USED (TSV05 ONLY)				

The first two words of the set Characteristics data packet give the address of the message buffer in CPU memory. The message packet buffer must reside on an even address boundary in CPU memory. If bit 0 of the first packet word (low order message buffer address) or bits 2-15 (extended features disabled) or bits 6-15 (extended features enabled) of the second packet word (high order message buffer address) are not zero, the command is rejected and no message packet is sent. However, if the IE bit was set in the command packet header word, an interrupt will be generated.

The third word of the data packet specifies the number of bytes of the message buffer. Only values of either decimal 14 or 16 (extended features enabled) are valid. If a byte count of less than 14 is specified, the command will be rejected. If too large a value is given, the default setting will be used. Default is 14 if extended features are disabled; 16 if extended features are enabled. Note that only the TSV05 supports message buffer lengths of 16 bytes.

Table 4-6 defines the control bits in the fourth word of the characteristics data packet—the characteristics mode data word. Table 4-7 defines the control bits in the fifth word—the extended characteristics data word—of the set characteristics data packet. Note that the fifth word is supported only by the TSV05 handler.

Table 4-6. Characteristics Mode Byte Bit Definitions

Bit	Name	Definition
00-03	—	Not Used.
04	ERI	Enable Message Packet Release Interrupts to the CPU: If this bit is 0, interrupts will not be generated when a Message Packet Release command is received by the coupler; upon recognition of the command, only Subsystem Ready (SSR) will be reasserted. If ERI is a 1, an interrupt will be generated.
05	EAI	Enable Attention Interrupts: When this bit is a 0, attention conditions, such as off-line, and on-line will not result in interrupts to the CPU. If set to a 1, interrupts will be generated once the coupler owns the message buffer.
06	ENB	Enable Skip Tape Marks Stop at BOT: This bit is meaningful only if the ESS bit is set. If the drive is at BOT, when a Skip Tape Marks command is issued and the first record seen is a tape mark, then the transport will set LET (XSTAT0) and stop after the first tape mark. If ENB is clear, the drive would not set LET but just count the tape mark and continue.
07	ESS	Enable Skip Tape Marks Stop: When set, the transport stops during a Skip Tape Mark command when a double tape mark (two contiguous tape marks) is detected. If cleared, the Skip Tape Marks command will terminate only on Tape Mark Count Exhausted or if BOT is detected.
08-15	—	Not Used.

Table 4-7. Extended Characteristics Data Word Bit Definitions (TSV05 Only)

Bit	Name	Description
0-4	—	Not Used.
5	HSD	High-Speed/High Density Select. 0 low density or start/stop 1 high density or stream
6-15	—	Not Used.

MESSAGE PACKET

The message packet format in the message buffer is used for all messages, whether at the end of a command or for an Attention. The message consists of a Header word, a Data Field Length word, a Residual Byte/Record/Tape-Mark Count word, and either four or five extended status registers. Normally, only four extended status registers are provided. The fifth one (XSTAT4) is available only when the extended features function of the coupler is enabled. This feature is supported only by the TSV05.

A summary of the message packet registers is shown at the end of ths section.

Message Packet Header Word

15	14 — 12	11 — 08	07 — 05	04 — 00
ACK	ALWAYS 0	ERROR CLASS CODE	ALWAYS 0	MESSAGE TYPE

ACK — ACKNOWLEDGE

Message Header Word Bit Definitions

Bit	Function
0-4	**Termination Code (TSSR)** / **Message Type** / **Definition** 0,2 — 10000 — End—no errors 3 — 10001 — Failure to execute 4,5,6,7 — 10010 — Error during execution (1 or more) 1,7 — 10011 — Attention. Interrupt caused by condition specified by error class codes.
5-7	Always Zero.
8-11	Error class codes—These bits define the class of failures found in the rest of the message buffer. **MSG Type** / **Class Code** / **Definition** ATTN — 0000 — Drive went on- or off-line (termination code = 10011) FAIL — 0001 — Other error (ILC, ILA, NBA) (termination code = 10001) FAIL — 0010 — Write lock error no non-executable function (termination code = 10001)
12-14	Always Zero.
15	This bit is used by the coupler to inform the CPU that the command buffer is now available for any pending or subsequent command packets. On an ATTN message, this bit will not be set.

Message Packet Data Field

15 — 04	03	02	01	00
ALWAYS 0	1	0	1	0

OCTAL 12 OR 14

This value follows the message header word in the message packet. This byte count represents the number of bytes remaining in the message packet. These bits always contain an octal 12 or 14 representing five or six words: the residual frame count and four or five status words (as specified through a previous Set Characteristics command).

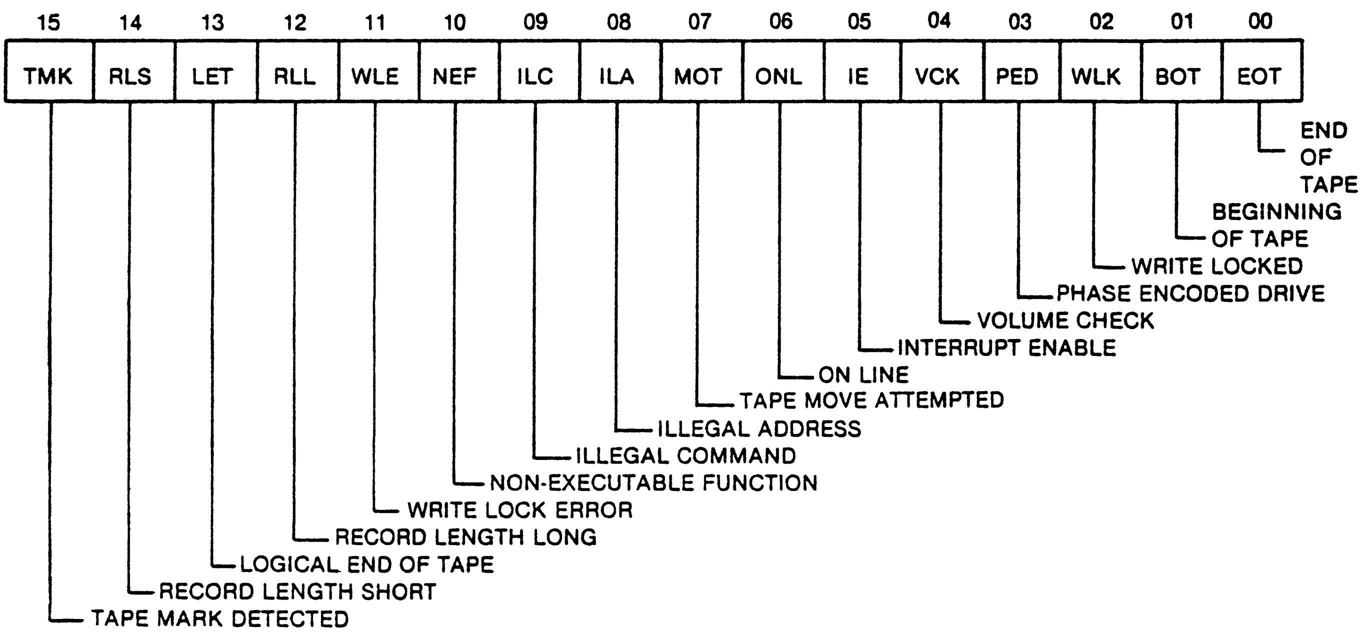
Residual Frame Count (RBPCR) Word

15	00
RESIDUAL FRAME COUNT WORD	

Word Three in the Message Packet

Bits	Description
00-15	This word contains the octal count of residual bytes, records, tape marks for the Read, Space Records, and Skip Tape Mark commands. The contents are meaningless for all other commands.

Extended Status 0 (XSTAT0) Word



Extended Status 0 Word Bit Definitions

Bit	Name	Termination Code (TC)	Definition
00	EOT	2	End of Tape: This bit is set whenever the tape is positioned at or beyond the end-of-tape reflective strip. It is not reset until the tape passes over the reflective strip in the reverse direction under program control. Subsystem initialization always resets this bit (status on read, TC2 on a write). Manually moving the EOT strip over the EOT sensor will not set or reset the EOT bit.
01	BOT	2/3	Beginning of Tape: When set, this bit indicates that the tape is positioned at the load point as denoted by the BOT reflective strip on the tape. This causes TC2 if reversed to BOT, and TC3 if at BOT when a reverse command occurs.
02	WLK	3	Write Locked: When set, this bit indicates that the mounted tape reel does not have a write enable ring installed. Therefore, the tape is write protected.

03	PED	—	Phase Encoded Drive: When set, this bit indicates that the transport is capable of reading and writing 1600 bit phase encoded data. When 0, this bit indicates 800 bpi, NRZ data.
04	VCK	3	Volume Check: This bit is set when the transport changes state (on-line to off-line and vice versa). It is always set after initialization.
05	IE	—	Interrupt Enable: This bit reflects the state of the Interrupt Enable bit in the last command.
06	ONL	1/3	On-Line: When set, this bit indicates that the transport is on-line and operational. It causes a TC1 on ATTN interrupt or a TC3 or a non-executable function if rejected because the transport was off-line.
07	MOT	—	Motion: Attempted to move tape.
08	ILA	3	Illegal Address: Address contains more than 18 bits or is an odd number.
09	ILC	3	Illegal Command: This bit is set when a command is issued and either its command code field or its command mode field contains codes not supported by the transport.
10	NEF	3	Non-Executable Function: When set, this bit indicates that the command could not be executed due to one of following conditions: • The command specified reverse tape direction but the tape was already positioned at BOT. • A motion command was issued without the Clear Volume Check (CVC) bit being set while the Volume Check bit was set. • A motion command was issued when the transport was off-line. • A write command was issued when the tape did not contain a write enable ring (Write Lock Status [WLS]).
11	WLE	3	Write Lock Error: When set, a TC3 indicates that a write operation was issued but the mounted tape did not contain a write enable ring.
12	RLL	2	Record Length Long: When set, this bit indicates that the record read was longer than the byte count specified.
13	LET	2	Logical End of Tape: This bit is set only on the Skip Tape Marks command under two conditions: when either two contiguous tape marks are detected or when moving off BOT and the first record encountered is a tape mark. This bit will not set unless this mode of termination is enabled through use of the Set Characteristics command. LET will set only in the forward direction.
14	RLS	2	Record Length Short: This bit indicates one of the following: 1) The record length was shorter than the byte count on read operations; 2) a space record operation encountered a tape mark or BOT before the position count was exhausted; 3) a Skip Tape Marks command was terminated by encountering BOT or a double tape mark (if Skip Tape Marks command is enabled (see LET, bit 13) before exhausting the position counter.
15	TMK	2	Tape Mark Detected: This bit is set when a tape mark is detected during a read, space, or skip command and as a result of the Write Tape Mark or Write Tape Mark Retry commands.

Extended Status 1 (XSTAT1) Word

15	14–09	08	07–02	01	00
DLT	NOT USED	RBP	NOT USED	UNC	PAR ER
DATA LATE				UNCORRECTABLE DATA	READ DATA PARITY ERROR

Extended Status 1 Word Bit Definitions

Bit	Name	Termination Class (TC) Octal Code	Definition
00	PARER	4	Read-Data Parity Error: When set, this bit indicates that the coupler has detected a parity error on the read-data lines coming from the transport.
01	UNC	4	Uncorrectable Data: This bit is set when either a parity error occurs without a corresponding dead track indicator, or more than one dead track occurs in either the preamble or the data field.
02-07	—	—	Always 0.
08	RBP	4	Read Data Parity Error: When set, this bit indicates that the coupler has detected a parity error on the read-data lines coming from the transport (TU80/TSV05).
09-14	—	—	Always 0.
15	DLT	4	Data Late: This bit is set when the FIFO is full on a read or empty on a write. These conditions occur whenever the UNIBUS latency exceeds the transport's data transfer rate for a significant number of transfers.

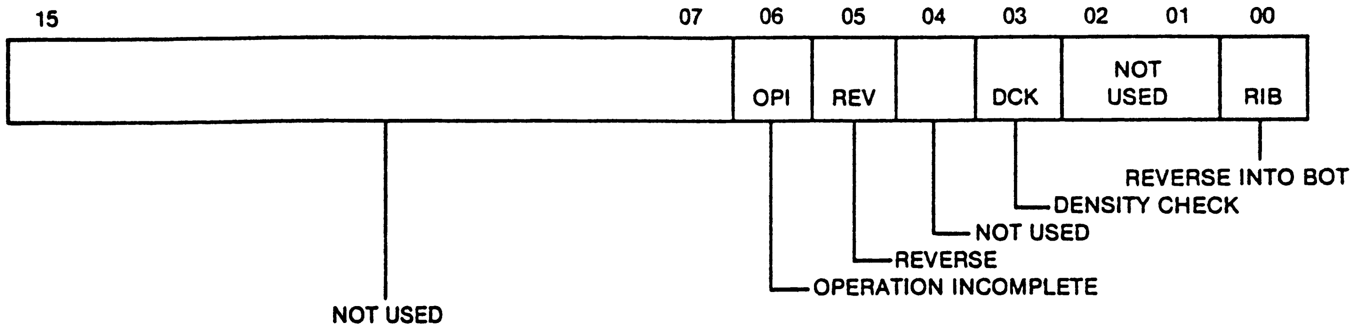
Extended Status 2 (XSTAT2) Word

15	14–08	07	06	05–00
OPM	NOT USED	XFS	0	FIRMWARE VERSION (SET CHARACTERISTICS CMD ONLY)
OPERATION ATTEMPTED TO MOVE TAPE				

Extended Status 2 (XSTAT2) Bit Definitions

Bit	Name	Termination Class (TC) Octal Code	Definition
00-05	S		Firmware Version Level: Valid if message is for a Set Characteristics command; zero otherwise.
06	—		Not Used (ALWAYS 0).
07	XFS	S	Extended Features Switch Setting (TSV05 Emulation)
08-14	—		ALWAYS 0.
15	OPM	S	Operation Moved Tape: When set, this bit indicates that the last command caused the tape to be moved.

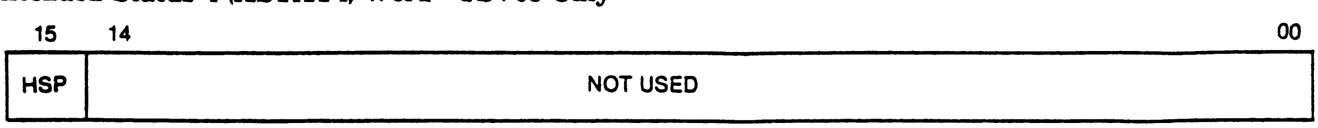
Extended Status 3 (XSTAT3) Word



Extended Status 3 (XSTAT3) Word Bit Definitions

Bit	Name	Termination Code (TC)	Definition
00	RIB	2	Reverse into BOT: This bit is set when a read, space, skip, or reverse command already in progress encounters the BOT marker when moving tape in the reverse direction. Tape motion will be halted at BOT.
01-02	—	—	Not Used.
03	DCK	6	When set, this bit indicates that an invalid Identification Burst (IDB), signifying that the tape was not written in PE, was sensed at BOT. However, the tape can still be read if the IDB is incorrect and the tape is actually written in PE. **Note** *If a tape with a bad IDB is appended, a termination code 6 will not occur until a write is attempted.*
04	—	—	Not Used.
05	REV	—	Reverse: This bit is set when the direction of current tape operation is reverse. For multifunction retry commands, if at least one of the commands is reverse, the bit is set.
06	OPI	6	Operation Incomplete: This bit is set when a read, space, or skip operation has moved 25 feet of tape without detecting any data on the tape. It is also set by a write command when the read head fails to see data transitions after four feet of tape have been moved.
07-15	—	—	Not Used.

Extended Status 4 (XSTAT4) Word—TSV05 Only



Extended Status Register 4 (XSTAT4) Bit Definition (TSV05 Only)

Bit	Name	Termination Class (TC) Octal Code	Definition
0-14	—	—	ALWAYS 0.
15	HSP	S	High Speed: When set, this bit indicates that the transport is operating in high speed mode or high density. When this bit is clear, the transport is operating in low speed mode or low density.

BUFFER OWNERSHIP AND CONTROL

To prevent the coupler from updating the Message Buffer while the CPU is reading it, or the CPU from updating the Command Buffer while the coupler is reading it, the concept of "ownership" is defined. Each buffer may be owned by either the coupler or the CPU, but not by both. Ownership of a buffer can be transferred only by the current owner.

There are four different combinations of transferring the two buffers in the two directions:

1. Command Buffer: CPU to Coupler, by the CPU.
2. Command Buffer: Coupler to CPU, by the Coupler.
3. Message Buffer: CPU to Coupler, by the CPU.
4. Message Buffer: Coupler to CPU, by the Coupler.

Table 4-8 describes the buffer transfer operations.

A Subsystem Initialize aborts any current operation and gives ownership of both the Command Buffer and the Message Buffer to the CPU.

BUFFER CONTROL ON ATTENTIONS (ATTN)

An Attention (ATTN) is enabled by the CPU by setting up the appropriate Characteristics Mode word on the Write Characteristics command. It allows the coupler to flag exceptional conditions (change in transport on-line/off-line status) when the coupler is in the Idle state (not executing a command). If an ATTN condition occurs and the coupler does not own the Message Buffer, the coupler will queue the ATTN internally. Then, when the CPU releases the Message Buffer on the next command (with the ACK bit set), the coupler will output the ATTN message with the ACK bit 0 in the message header word to indicate that the command was lost (except for the transference of ownership of the Message Buffer to the coupler). In this case, the coupler refuses to accept ownership of the Command Buffer. The CPU will then still own the Command Buffer (because the coupler did not accept the command) and will also own the Message Buffer now filled with an ATTN message. If the CPU still wants to do the ignored command, the CPU must reissue the command (with the ACK bit set).

Table 4-8. Buffer Ownership Transfers

Buffer	Direction	Transfer Method
Command Buffer	CPU to Coupler	The CPU transfers ownership of the Command Buffer to the coupler by writing the address of the Command Buffer into the TSDB register. This clears the SSR bit in TSSR.
Command Buffer	Coupler to CPU	The coupler transfers ownership of the Command Buffer back to the CPU by depositing a Message Packet (in the Message Buffer) that has the Acknowledge (ACK) bit set in the message header word. After the message is deposited by the coupler, it sets the SSR bit in TSSR to indicate that the message is in the Message Buffer. If the message does not contain the ACK bit set, the CPU will know that the coupler did not see the last Command Buffer and that the CPU still owns the Command Buffer. The command may be reissued by the CPU (with the ACK bit set).
Message Buffer	CPU to Coupler	The CPU transfers ownership of the Message Buffer to the coupler by setting the ACK bit in the Command Buffer and then initiating the command by writing into TSDB. If the Command Buffer does not contain the ACK bit, the coupler will know that the CPU did not see the last message buffer and the coupler still owns it. The coupler, in response to the CPU writing into TSDB, will set SSR and perform an Interrupt (if the IE bit is set) without sending out a message, since it does not own the buffer.
Message Buffer	Coupler to CPU	The coupler transfers ownership of the Message Buffer to the CPU by writing the Message Buffer and setting the SSR bit. This can happen at one of two times: 1. At the end of a command, or 2. By outputting an Attention (ATTN) message. In this case, SSR will already be 1 because an ATTN only happens when the coupler is inactive. So the coupler clears SSR, outputs the message, then sets SSR again (and interrupts if the IE bit was set on the Message Buffer Release command that gave control of the Message Buffer to the coupler). Note that for an ATTN to occur, the EAI bit must have been set in the previous Write Characteristics command.
During normal command processing, the ownership of both buffers passes simultaneously, first from CPU to coupler (at the start of command processing, when the CPU writes a Command Pointer into the TSDB register), and then from coupler to CPU (upon completion of the command) when the coupler sets SSR in the TSSR.		

Now consider the case in which the CPU wants to be notified of a change in status while the coupler is inactive for a long period of time. To accomplish this, the coupler must own the Message Buffer for that entire period of time. Normally, the coupler gives up ownership of the Message Buffer at the end of a command. However, for enabling Attention messages, ownership of the Message Buffer is transferred to the coupler via the Message Buffer Release command. This is a special command that tells the coupler not to give ownership of the Message Buffer back to the CPU at the end of the command.

The coupler does not output a message at the end of this command, but just updates the TSSR register (with the SSR bit set) and interrupts (if the IE bit was set in the command and such an interrupt was enabled by the ERI bit in the previous Write Characteristics command). The coupler then maintains ownership of the Message Buffer until an ATTN condition is seen and then immediately clears SSR, outputs the ATTN message (with the ACK bit not set since the coupler is not responding to a command), and then sets SSR and interrupts the CPU (if the IE bit was set on the Message Buffer Release command). In this condition, the CPU owns the Command Buffer and the Coupler owns the Message Buffer. If the coupler outputs an Attention message, ownership of the Message Buffer is passed to the CPU. At that time the system is back to the state of the CPU owning both buffers. Another ATTN will not be done until the CPU does a command with the ACK bit set to release ownership of the Message Buffer containing the ATTN message.

If the CPU has done a Message Buffer Release command, and wants to do another command but has not received an ATTN from the coupler (so that the coupler still owns the Message Buffer from the Message Buffer Release command), the CPU can do a command without the ACK bit set in the command buffer. At the time the command is issued, the CPU does not own the Message Buffer so the CPU cannot release the Message Buffer. If the CPU does set the ACK bit, nothing will happen except that the CPU might miss an ATTN if the coupler was sending out an ATTN message at the same time that the CPU was issuing the command.

It is possible that the CPU may attempt to initiate a new command at or near the same time that the coupler attempts to output an Attention message. (The command must not have the ACK bit set since the CPU does not own the Message Buffer.) If the CPU writes the TSDB register while SSR is clear during an ATTN, the Register Modification Refused (RMR) error bit will be set and that command will be ignored. The ATTN message will not have the ACK bit set since the coupler does not own the Command Buffer. Note that RMR may set in this way on a bug-free system. All other settings of RMR indicate a software bug (the CPU tried to do a command before the previous command was finished). If the CPU command was lost because the coupler was outputting an ATTN message, Volume Check (VCK) and Interrupt Enable (IE) are not updated. If the CPU command was rejected (illegal command, etc.) and not ignored, VCK and IE are updated to the start of the rejected command.

MISCELLANEOUS STATUS AND ERROR HANDLING

The following points should be noted in regard to status and error handling:

1. Error bits in the TSSR register (SC and RMR) are cleared by successfully loading a command pointer into the TSDB register and by successfully depositing an END message.
2. All commands clear the internal copy of each error bit in the Extended Status registers. Therefore, a Get Status command will not return the error bits as set up by a previous tape operation.
3. A read operation which encounters a tape mark will not transfer any data and will give a Tape Status Alert termination. The Tape Mark and Record Length Short status bits will be set, and the RBPCR word in the message buffer will contain the original byte count as specified in the command.
4. A Space Records operation will automatically terminate when a tape mark is traversed, and the TMK status bit will be set. Also, Record Length Short (RLS) will be set if the record count was not decremented to zero.
5. A Skip Tape Marks operation will automatically terminate when two consecutive tape marks are encountered and the "Enable Skip Stop" (ESS) mode is enabled via the Write Characteristics command. Record Length Short (RLS) will be set if the count was not decremented to zero. The same is also true if a tape mark is the first record off BOT and both the ESS and ENB bits were set in the previous Write Characteristics data word.
6. Every Write, Write Retry, Write Tape Mark, Write Tape Mark Retry, and Erase command which is executed at or beyond the EOT marker will result in a Tape Status Alert termination. The internal EOT status bit will remain set until logically passed over in the reverse direction (Rewind, Reverse Read,

Reverse Space, etc.). The EOT status bit is not specifically identified with a particular record.

7. A Read Reverse, Space Reverse, Reverse or Skip Tape Marks Reverse command which encounters BOT after the operation is underway will result in a Tape Status Alert termination (the RIB status bit will be set).

8. If a Read Reverse, Space Records Reverse, or Skip Tape Marks Reverse command is issued while the tape is already at BOT, a Function Reject (NEF-Non-Executable Function) status will be returned.

9. When a normal rewind command is issued, the termination message and interrupt will not occur until the tape reaches BOT and has stopped. If the tape is already at BOT when the command is issued, the transport will still be commanded to rewind to make sure the tape is properly positioned.

10. When a Rewind with Immediate Interrupt command is issued, the coupler commands the transport to rewind, checks for proper status, and then issues an Interrupt and END message for normal termination. If a new tape motion command is issued to a rewinding unit, the coupler will wait until the tape has been rewound to BOT before proceeding with the new command. During execution of a Rewind with Immediate Interrupt, the Motion (MOT) bit in XSTAT0 will be set if a Get Status command is performed.

11. Any write function issued at BOT (including Erase) which results in the Density Check bit (DCK) being set will cause a termination of that command with a TSSR Termination Class code of 6 set to indicate an unrecoverable error. Normally, a write function causes the PE Identification (ID) burst to be written off BOT, and the coupler checks for the appropriate signal from the transport. Therefore, if DCK is set on a write off BOT, a serious transport or coupler problem exists.

12. If a Density Check condition is detected during a read, space or skip function, the DCK bit will be set but the operation will not be aborted. If DCK is the only error status bit set during the operation, normal termination will be reported. This allows tapes with good data but bad density check (ID) areas to be read. If, in fact, a tape of the wrong density has been mounted, other errors will be reported and will stop the operation.

13. Note that if you begin reading a tape, get a Density Check with no other errors, and then append data to the tape, the write command will get a Termination Class code of 6, indicating that tape position is lost, because Density Check will remain set. The whole tape should be copied over so that drives that depend on the ID burst will be able to read the tape.

14. Certain failures can result in no interrupt even though the specified command had Interrupt Enable set. These failures include NXM (Non-Existent Memory Error), since the failure could have occurred before the Interrupt Enable bit was fetched from the command packet.

15. The software should defend against unexpected interrupts, since the tape subsystem may not be useable, but the software should still not crash.

BIT POSITION	15 (MSB)	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00 (LSB)

STATUS REGISTER (TSSR) 772522 (Transport 0) 772526 (Transport 1) 772532 (Transport 2) 772536 (Transport 3)	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	SC			RMR	NXM	NBA	A17	A16	SSR	OFL			TC2	TC1	TC0	

MESSAGE PACKET HEADER WORD (STATUS ADDRESS)	15	14–12	11–08	07–05	04–00
	ACK	ALWAYS 0	ERROR CLASS CODE	ALWAYS 0	MESSAGE TYPE

MESSAGE PACKET DATA FIELD	15–04	03	02	01	00
	ALWAYS 0	1	0	1	0

RESIDUAL FRAME COUNT (RBPCR) WORD (STATUS ADD + 4)	15–00
	RESIDUAL FRAME COUNT WORD

EXTENDED STATUS 0 (XSTAT0) WORD (STATUS ADD + 6)	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	TMK	RLS	LET	RLL	WLE	NEF	ILC	ILA	MOT	ONL	IE	VCK	PED	WLK	BOT	EOT

EXTENDED STATUS 1 (XSTAT1) WORD (STATUS ADD + 8)	15	14–09	08	07–02	01	00
	DLT	NOT USED	RBP	NOT USED	UNC	PAR ER

EXTENDED STATUS 2 (XSTAT2) WORD (STATUS ADD + 10)	15	14–08	07	06	05–00
	OPM	NOT USED	XFS	0	FIRMWARE VERSION (SET CHARACTERISTICS CMD ONLY)

EXTENDED STATUS 3 (XSTAT3) WORD (STATUS ADD + 12)	15–07	06	05	04	03	02–01	00
	NOT USED	OPI	REV	NOT USED	DCK	NOT USED	RIB

EXTENDED STATUS 4 (XSTAT4) WORD (EXTENDED FEATURES MODE) TSV05 ONLY	15	14–00
	HSP	NOT USED

Figure 4-3. Message Packet Summary of Registers

BLANK

SECTION 5
TROUBLESHOOTING AND THEORY

This section describes troubleshooting procedures at three levels of complexity: basic system, coupler symptoms and detailed analysis. Basic system troubleshooting procedures are visual checks not requiring test equipment and may be performed by the operator. Coupler symptom procedures may require a scope, meter, extender board or diagnostics and should be performed by a technician. Detailed analysis is troubleshooting at the IC level, and is presented for engineers or system analysts for coupler evaluation. The latter method may require the use of test equipment and the material presented here: board layout, term listing, theory of operation and logic diagrams.

CAUTION

Any troubleshooting requires a familiarity with the installation and operation procedures in this manual, the appropriate DEC manual, and the tape drive manufacturer's manual. Ensure power is off when connecting or disconnecting the board or plugs.

BASIC SYSTEM TROUBLESHOOTING

The following should be checked before power is applied:

1. Verify that all signal and power cables are properly connected. Ribbon cable connectors are *not* keyed. The arrows on the connectors should be properly aligned.

2. Verify that all modules are properly seated in the computer and are properly oriented.

The following should be checked during or after application of power:

1. Verify that the computer and tape drive generate the proper responses when the system is powered up.

2. Verify that the computer panel switches are set correctly.

3. Verify that the console can be operated in the local mode. If not, the console may be defective.

4. Verify that the green diagnostic light on the coupler is on.

COUPLER SYMPTOMS

Coupler symptoms, possible causes and checks/corrective action are described in Table 5-1. Voltage checks should be performed before troubleshooting more complex problems. The +5V source may be checked from any component shown on the other logic diagrams.

PHYSICAL LAYOUT

The physical layout of the board is shown in Figure 5-1. Column and row numbers on the layout correspond to the numbers on each IC on the logic diagrams.

TERM LISTING

The input and output terms for each logic diagram are described in Table 5-2. The sources and destinations refer to the sheet numbers of the logic diagrams.

Table 5-1. Coupler Symptoms

Trouble	Possible Cause	Check/Replace
1. GREEN DIAGnostic light on coupler is OFF.	1. Microprocessor section of coupler inoperative. a. Short or open on board. b. Bad integrated circuit. c. No DC power.	1. Coupler. Put board on extender. With scope look at pins of 2901. All pins except power and ground should be switching. Look for "stuck high", or "stuck low", or half-amplitude pulses. If no switching, either power or crystal bad.
2. No communication between console and computer.	2. I/O section of coupler "hanging up" Q Bus. a. BREQ− always low. b. Shorted bus transceiver IC. c. Bad CPU board.	2. Computer interface logic of coupler. a. Check signal BREQ− for constant assertion. b. Check I/O IC's. Remove coupler board to see if trouble goes away. c. Run CPU diagnostics.
3. No data transfers to/from tape.	3. Tape not ready or bad cable connection. a. Improper communication with tape registers on coupler or bad IC in register section of coupler.	3. Check tape switches and cable connector. a. Load and read tape registers from console with processor halted. Verify bits loaded can be read.
4. Data transferred to/from tape incorrect.	4. Bad memory board in backplane. a. Noise or intermittent source of DC power in computer. b. Bad IC in tape I/O section of coupler. c. Run tape diagnostic, set console to make system 'Halt On Error." d. Bad area on tape. e. Head worn.	4. Run memory diagnostics. a. Check AC and DC power. b. While operating, check lines from coupler to tape with a 'scope for short or open. c. Analyze error halt. d Errors should always occur in the same sector of tape. e. Replace head.

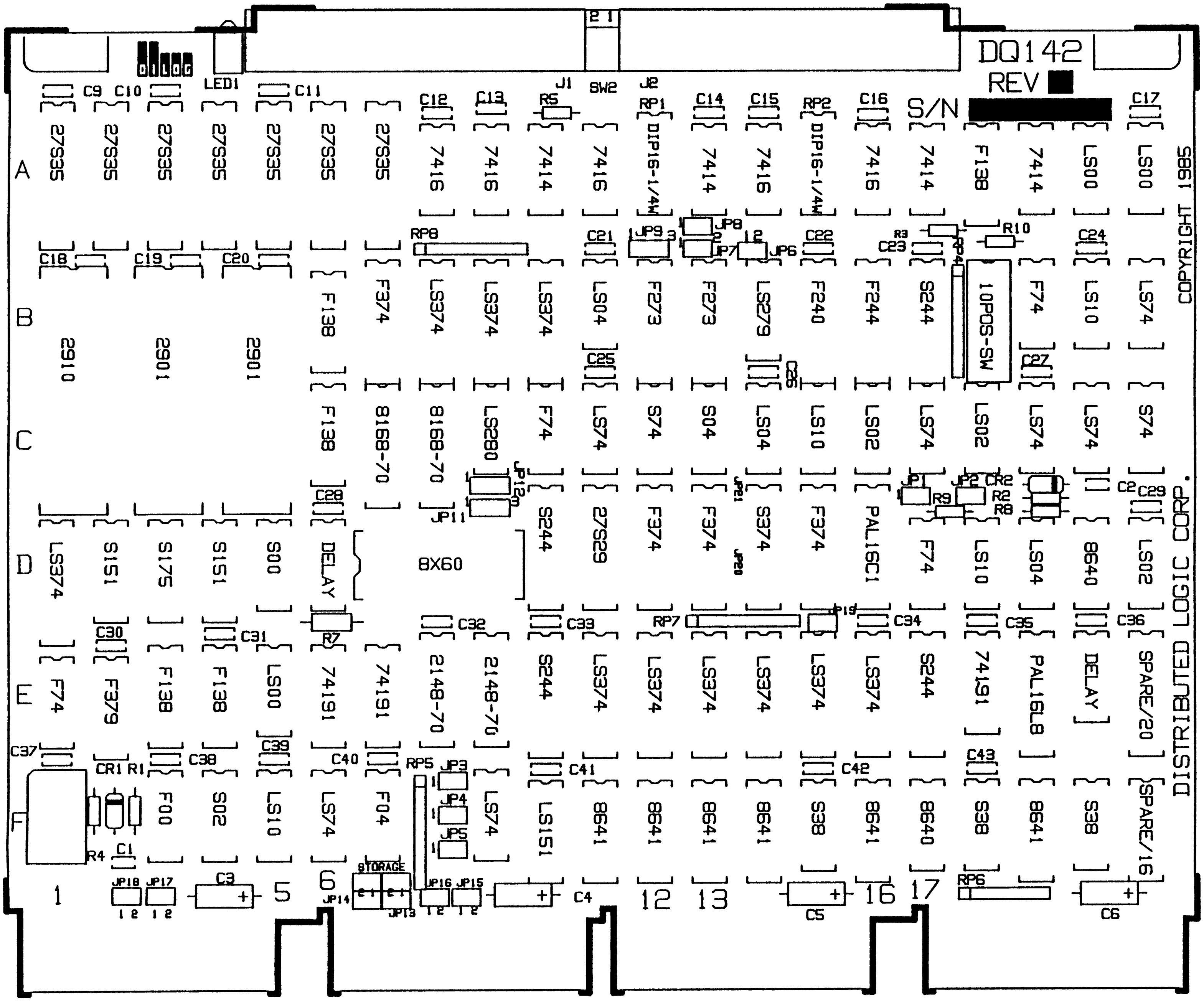


Figure 5-1. Board Layout

Table 5-2 Term Listing

Term	Origin Sheet	Description
ACK−	13	Acknowledge
ADDOVFL+	2	Address Overflow
BBS7L	5	Bus Bank Select 7
BDAL0L-	2	Bus Data/Address Lines 0-7 (Least
BDAL7L		Signficant Byte)
BDAL8L-	3	Bus Data/Address Lines 8-15 (Most
BDAL15L		Significant Byte)
BDAL16L-		
BDAL21L	3	Extended Bus Address Lines
BD0+-	2,3	Buffered Data/Address Lines
BD15+		Internal to Coupler from Q Bus
BDCOKH	4	Bus DC Power OK
BDINL	4	Bus Data In
BDMG1IL	6	Bus Direct Memory Grant 1 In
BDMG1OL	6	Bus Direct Memory Grant 1 Out
BDMRL	6	Bus Direct Memory Request
BDOUT	4	Bus Data Output
BIAK1IL	7	Bus Interrupt Acknowledge In
BIAK1OL	7	Bus Interrupt Acknowledge Out
BINITL	4	Bus Initialize
BIRQ4,5,6,7	7	Bus Interrupt Request Piority Lines
BREQ	13	Bus Request from Microprocessor
BRPLYL	5	Bus Reply
BSACKL	6	Bus Select Acknowledge
BSYNCL	4	Bus Synchronize
BWTBTL	4	Bus Write Byte
CCE−	9	Condition Code Enable
CCG+	15	PE/NRZI Detect Signal
CIN	12	Carry In to 2901
CLEAR	5	Clear (Reset) Signal for Coupler
CLREOT	13	Clear End of Tape
COUT	12	Carry Out of 2901
CRI-0/7	11	Control Register One Bits 0-7
CR2-0/7	11	Control Register Two Bits 0-7
CR3-0/7	11	Control Register Three Bits 0-7
CR4-0/7	11	Control Register Four Bits 0-7
CR5-0/7	11	Control Register Five Bits 0-7
CR6-0/7	11	Control Register Six Bits 0-7
CSA0+/	10	Control Store Address Bits
CSA9+		Zero Through Nine
DATLAT−	16	Data Late
DCOK+	4	DC Power OK
DEMAND+	5	Demand Bus Cycle
DMATIME−	6	DMA Transfer Time
DONE+	6	DMA Transfer Done
D00+/D07+	4,5,8, 11,14, 15,17	8-Bit D Bus Lines Input to 2901
EADD−	6	Enable Address
EDATA−	6	Enable Data
EIFACE−	6	Enable Interface to Q Bus
EMPTY+	16	FIFO is Empty
ENFIFO	16	Enable FIFO
EOTSTA+	15	End of Tape Status
ERASE+	15	Erase Tape Interface Signal
FAD0/FAD9	16	FIFO Address Bits 0-9 (10 Bits)
FCCG/ID	15	Formatter Identification Burst
FCER	15	Formatter Corrected Error
FDBY	15	Formatter Data Busy
FDEN	15	Formatter Density
FEDIT	15	Formatter Edit
FERASE	15	Formatter Erase
FEOT	15	Formatter End of Tape
FFAD	15	Formatter Address
FFBY	15	Formatter Busy
FFEN	15	Formatter Enable
FFMK	15	Formatter File Mark
FFPT	15	Formatter File Protect
FGO	15	Formatter Go
FHER	15	Formatter Hard Error

Table 5-2. Term Listing (Continued)

Term	Origin Sheet	Description
FIFRD−	16	FIFO Read
FIFWT−	16	FIFO Write
FLDP	15	Formatter Load Point
FLOL	15	Formatter Load On Line
FLWD	17	Formatter Last Word
FNRZ	14	Formatter Non Return to Zero
FOFL	15	Formatter Off Line
FONL	15	Formatter On Line
FRD0-FRD7	17	Formatter Read Data Bits 0-7
FRDY	15	Formatter Ready
FRDP	17	Formatter Read Data Parity Bit
FREV	15	Formatter Reverse
FREW	15	Formatter Rewind
FRTH1,2	15	Formatter Read Thresholds 1 and 2
FRWD	15	Formatter Rewinding
FTAD0,1	15	Formatter Transport Address 0,1
FULL	16	FIFO Full
FWD0-7	17	Formatter Write Data Bits 0-7
FWDP	17	Formatter Write Data Parity Bit
FWFM	15	Formatter Write File Mark
FWRT	15	Formatter Write
GPUA	4	Ground Pull Up A . . .
INACT+	16	Input to FIFO Active
INCRAM−	13	Increment RAM
INTIME	7	Data Being Read In
LCOUT+	9	Latched Carry Out
LDDIR	6	Load Data Input Register
LOROM	8	Load Output of ROM
LXRB	13	Load Micro Vector Address
LXRC	13	Load Self Test Flip-Flop (LITE)
LXRD	13	Load ROM Address
LXRE	13	Load RAM Address
LXRF	13	Load RAM Destination
LXR0	13	Load Data Output Register (MSB)
LXR1	13	Load Data Output Register (LSB)
LXR2	13	Load DMA Address (MSB)
LXR3	13	Load DMA Address (LSB)
LXR4	13	Load DMA Address (EXT)
LXR5	13	Load Transport Command Register
LXR6	13	Load FIFO Buffer
LXR7	13	Load Transport Control Register
LXR9	13	Enable FIFO
OUTACT	16	Output of FIFO Active
PARER+	17	Parity Error
RBYTE	4	Write Byte (Received)
RDIN	4	Data In (Received)
RDMR	6	Direct Memory Request (Received)
RDOUT+	4	Data Out (Received)
RELBUS	13	Release Bus
RESET	4	Reset—BDCOK, INIT, or Power-Up
RRPLY+	5	Reply (Received)
RSTR+	16	Read Strobe
RSYNC+	4	Synchronize (Received)
RWTBT	4	Write Byte (Received)
SCLK	8	System Clock: 166.6 nsec
SETEOT	13	Set End of Tape
STDMA	13	Start DMA
STLGOOD	8	Self Test is Still Good
TBYTE+	3	Transmit Byte
TDIN	6	Transmit Data In
TDOUT	6	Transmit Data Out
TRPLY	5	Transmit Reply
TSYNC	6	Transmit Synchronize
TWRITE+	3	Transmit Write
TWTBT−	6	Transmit Write Byte
VEC+	10	Vector Enable
WRT	15	Write to Formatter
XCLK−	8	Register Clock
XSDA	13	External Source Literal Select
XSDD	13	External Source Switches 2 Select

Table 5-2. Term Listing (Continued)

Term	Origin Sheet	Description
XSDE	13	External Source ROM Select
XSDF	13	External Source RAM Select
XSD0	13	External Source Slave Address Select
XSD1	13	External Source Data Input (MSB) Select
XSD2	13	External Source Data Input (LSB) Select
XSD3	13	External Source CPU Bus Status Select
XSD4	13	External Source FIFO Buffer Select
XSD7	13	External Source Transport Status 1 Select
XSD8	13	External Source Transport Status 2 Select
XSD9	13	External Source Switches 1 Select
Y00/Y07	12	8-Bit Y Bus from 2901
ZERO+	12	Zero Result Output of 2901

THEORY

The coupler may be examined as three parts: computer interface, formatter interface and coupler internal functions. Signals from and to the computer are described in Section 1, Table 1-1. Signals from and to the formatter are described in Table 1-2. Figure 5-2 is a simplified block diagram illustrating the interfaces and listing the major functional components. Single lines in the illustration represent serial data and the wide lines represent parallel data. A detailed block diagram of the coupler is shown on Sheet 1 of the logic drawings. The numbers in the blocks on Sheet 1 refer to the sheet numbers of the other logic diagrams.

Computer Interface

The purpose of the computer interface is to (1) buffer lines between the Q Bus of the computer and the coupler and (2) synchronize information transfers. There are two major classes of lines connected to the computer interface:

a. Data/address lines

b. Control lines

There are 16 bidirectional data/address lines and six extended address lines. Both device addresses and data are transferred over these lines. Address information is first placed on the lines by a bus master. The bus master then either receives input data from, or outputs data to, the addressed slave device, or memory, over the same lines. During initial control and status-transfer sequences, the coupler is a slave device. During data transfers, the coupler is a bus master and either receives data from, or outputs data to, the processor memory via the DMA facility.

The control lines request information transfers, select the type and direction of transfers, and synchronize the transfers. The control lines are functionally unidirectional and originate either at the processor or at the coupler.

The computer interface controls the synchronization, or "bus arbitration" sequence. Bus synchronization is done by a separate hardware state processor, rather than by the microprocessor, to minimize bus use by the coupler. This permits the tape coupler and many other devices to use the DMA channel efficiently on a time multiplexed basis.

Microprocessor

A bit-slice microprocessor with an internal 8-bit bus is the timing and control center of the coupler. The microprocessor is controlled by instructions stored in Programmable Read Only Memory (PROM). These instructions, called firmware, cause the microprocessor to operate in a prescribed sequence.

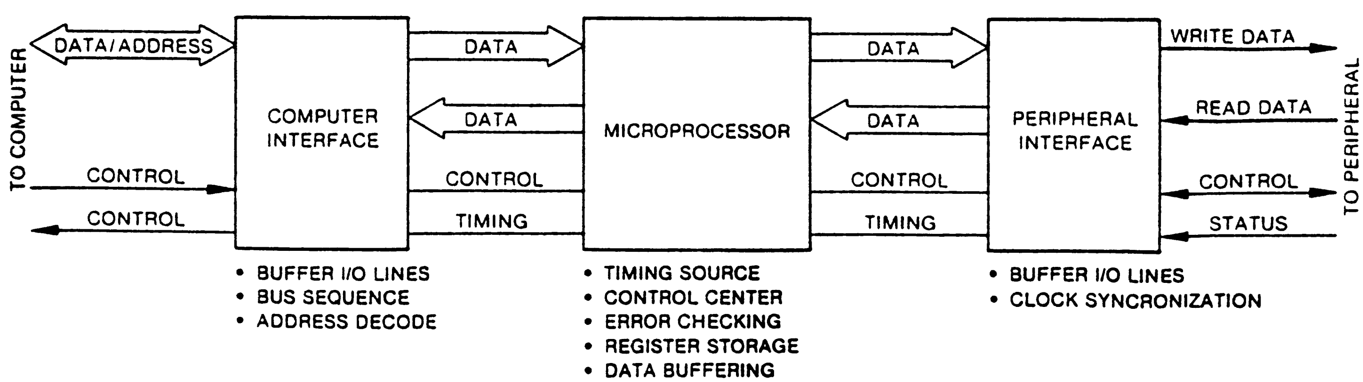


Figure 5-2. Simplified Block Diagram Tape Coupler

The Q Bus hardware registers (TSDB/TSBA and TSSR) reside in a 256-byte RAM which is also used by the microprocessor to buffer up to 8 bytes of data during DMA transfers, store command packets, and store status and errors used in assembling message packets. The DMA buffer in RAM, in conjunction with a 4096 x 8-bit FIFO RAM data buffer and two hardware byte registers in the peripheral interface, provide a total of up to 4106 bytes of data buffering between the drive interface and the Q-Bus, all but completely eliminating the likelihood of errors (a byte of data can be considered the equivalent of a character). An on-board 512-byte table PROM increases overall efficiency by aiding the microprocessor in processing errors and status.

Peripheral Interface

The purpose of the peripheral interface is to permit communication between the coupler and tape drive. The peripheral interface comprises:

A. Line drivers and receivers that buffer the data, status, and control lines between the coupler and the tape drive formatter over cable lengths of up to 25 feet,

B. Jumpers and switches permitting flexibility in tape subsystem configurations,

C. A 4K x 8-bit FIFO data buffer between the coupler and the tape drive.

Computer Interface

The computer interface comprises the following logic elements:

A. Data/address registers and receivers/drivers

B. Extended address register and receivers/drivers

C. Address decode logic

D. Control receivers/drivers

E. Status and control logic

F. Jumpers and switches permitting flexibility in CPU system configuration

The computer interface is a hard-wired logic section that buffers and synchronizes information transfers over the Q Bus between the coupler and another device. The address decode logic dynamically monitors the Q-Bus address lines. When the address of the TSDB/TSBA or TSSR/TSDBX register associated with the coupler is asserted or a bus request has been granted, the status and control logic is enabled, alerting the microprocessor to a bus cycle requiring immediate servicing.

Address Decode Logic (Sheet 5)

The address decode PAL (16D) enables flip-flop 17D-9 to be set by RSYNC+ if one of the coupler addresses is detected. One of four possible blocks of addresses can be selected by the jumpers JP1 and JP2 connected to pins 1 and 19 of PAL 16D. (See Section 2 for address selection.) Up to four logical units (four pairs of registers) can be accessed within each address block, depending upon how many units are enabled by switches S9 and S10.

Additional inputs to the address decode logic are the 13 least significant address bits from the Bus data/address register and receivers/drivers (Sheets 2 and 3) and the BBS7L signal from the Q Bus.

The four least significant address bits are gated to the D Bus by XSD0− through circuit 14D, which is the "decode slave address" signal from the D-Bus source decode logic (Sheet 13).

Data/Address Register Receivers/Drivers (Sheets 2, 3, 4)

The 16 data and least significant address bits are buffered between the Q Bus and the coupler Y Bus by circuits 16F, 14F, 12F and 13F shown on Sheets 2, 3 and 4; the six most significant address bits are buffered by circuits 15F and 20F (Sheet 3) and originate at output register 15E (Sheet 3). Signal EADD− connects address bits from the coupler Y Bus to the Q Bus. The byte-wide Y-Bus is strobed into the 22-bit-wide address bus by signals LXR0, LXR1, LXR2, LXR3 and LXR4.

Note that three of the four least significant Y-Bus bits are connected through up/down counter 18E to data/address bus transceiver circuit 16F. This up/down address counter automatically updates the address after each DMA. When the DMA address rolls over a quad-word boundary, signal ADD0VFL+ is activated, signaling the microprocessor to update the upper address bits.

Received data/address lines are labeled BD0-BD15. The received data signals are latched into receiver registers 13D, 15D by LDDIR− and connected to the D Bus by XSD1− and XSD2−. Data from the Y Bus is stored in data driver registers by LXR0− and LXR1− and enabled onto the Q Bus by EADD− and EIFACE−.

Bus Control Receivers/Drivers (Sheets 4, 5, 6, 7)

The control lines of the Q Bus are buffered on the coupler by circuits 19F, 18F, 20F, 17F and 11F. Bus control drive circuit 19F is enabled by DMATIME− and circuit 11F is enabled by the BREQ− signal.

The jumpers shown on Sheet 4 permit the coupler to be used in any slot of a MicroVAX backplane. See Section 2.

Bus Status and Control Logic (Sheets 5, 6, 7, 8)

To minimize time on the bus, bus transfers are handled mostly by hard-wired logic with very little intervention by the microprocessor. Information transfers are of two kinds: programmed I/O and direct to memory (DMA). During programmed I/O transfers the processor is bus master with the coupler as slave. During DMA transfers the coupler is bus master with memory as slave.

The bus status and control logic comprises: A) controller bus request/grant logic (Sheet 7), B) DMA logic (Sheet 6), C) timing, status and self-test logic (Sheet 8), and D) slave reply logic (Sheet 5).

The crystal-controlled time base for the coupler is established by a 16 MHz oscillator (Sheet 8) whose output is divided by two by flip-flop 1E-9 to generate symmetrical 125-nanosecond clock signal SCLK−.

Clock signal XCLK is generated a few nanoseconds before SCLK to guarantee the external source select registers will store the contents of the Y Bus before the microprocessor is clocked to its next state.

Self-test latch IE-5 controls the diagnostic light and supplies the STLGOOD+ signal via the Q-Bus status register to the D-Bus. A loss of power to the controller (DCOK+ goes false) immediately clears IE-5. Flip-flop 1E-9 sets if the coupler passes self test (XLR0, YO0).

Bus control lines to the coupler, as well as some internal status conditions, are stored by buffered register 12D and connected to the microprocessor D-Bus by XSD3−.

The controller interrupt logic is shown on Sheet 7 and the DMA control logic is shown on Sheet 6.

Note that both interrupts and DMA transfers must be preceded by a request sequence to permit the coupler to become bus master.

For a detailed discussion of Q-Bus timing and control, review the LSI-11 Bus section of the DEC microcomputers handbook.

Bus Transfer Timing

Bus transfers are divided into the following operations:

- Data Input Transfer (DAT1) as slave (Programmed I/O)
- Data Output Transfer (DAT0) as slave (Programmed I/O)
- Data Input Transfer (DAT1) as master (DMA)
- Data Output Transfer (DAT0) as master (DMA)
- Interrupt Vector Transfer

Programmed I/O transfers are initiated with the coupler when the computer places the device address of the coupler on the BDAL00 through BDAL15 lines, asserts the BBS7L signal, and asserts signal BSYNCL. Within the coupler, BSYNCL converts to RSYNC.

Address decoder 16D monitors the address lines. When the coupler address is decoded and RSYNC is asserted, the 17D-9 flip-flop sets. This informs the microprocessor of an I/O register transfer (programmed I/O) that needs servicing.

The sequence for a DATI operation is shown in Figure 5-3. The coupler responds to input requests by asserting BRPLY within 10 microseconds of a

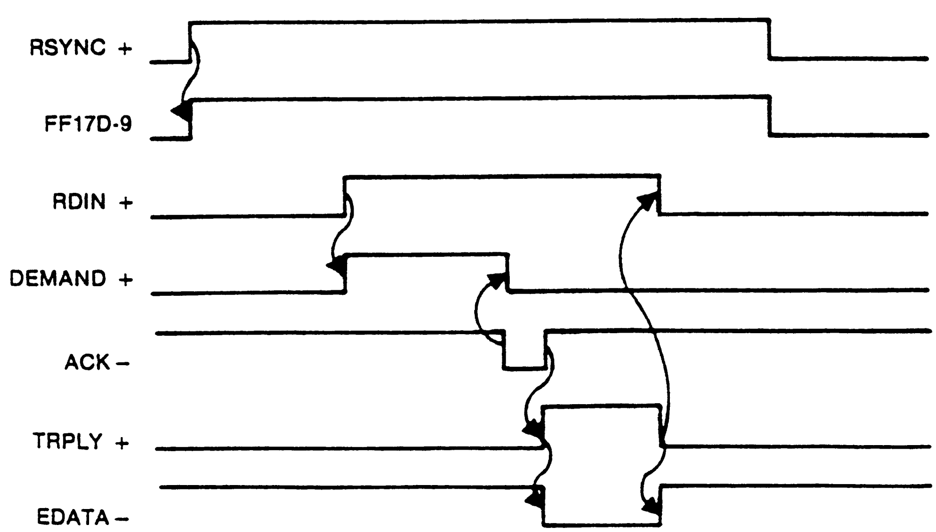


Figure 5-3. Q Bus DATI Transfer (Coupler as Bus Slave)

DATI request. DATI operations read the coupler I/O registers.

The sequence for a DATO operation is shown in Figure 5-4. DATO operations write to the coupler I/O registers.

DMA transfers are between the coupler and computer memory. The coupler is always bus master. There are two DMA transfer types: data into the coupler (DATI) and data out of the coupler (DATO). Once the coupler has been granted DMA bus control, the transfer sequence is similar to I/O bus transfers, except that now it is bus master.

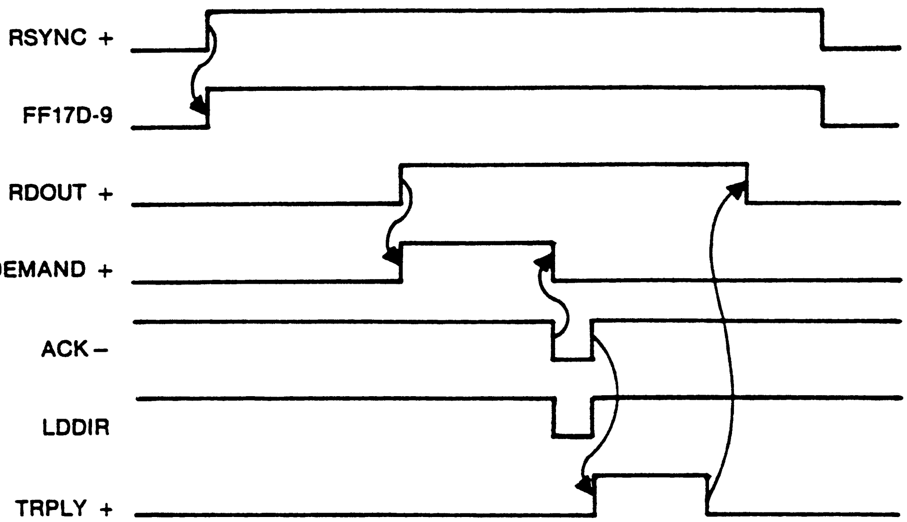


Figure 5-4. Q Bus DATO Transfer (Coupler as Bus Slave)

Figure 5-5 illustrates the DMA DATI timing (coupler as bus master); Figure 5-6 illustrates the DMA DATO timing.

Interrupt vector transfer timing is illustrated by Figure 5-7. Interrupt requests are originated by control pulse BREQ.

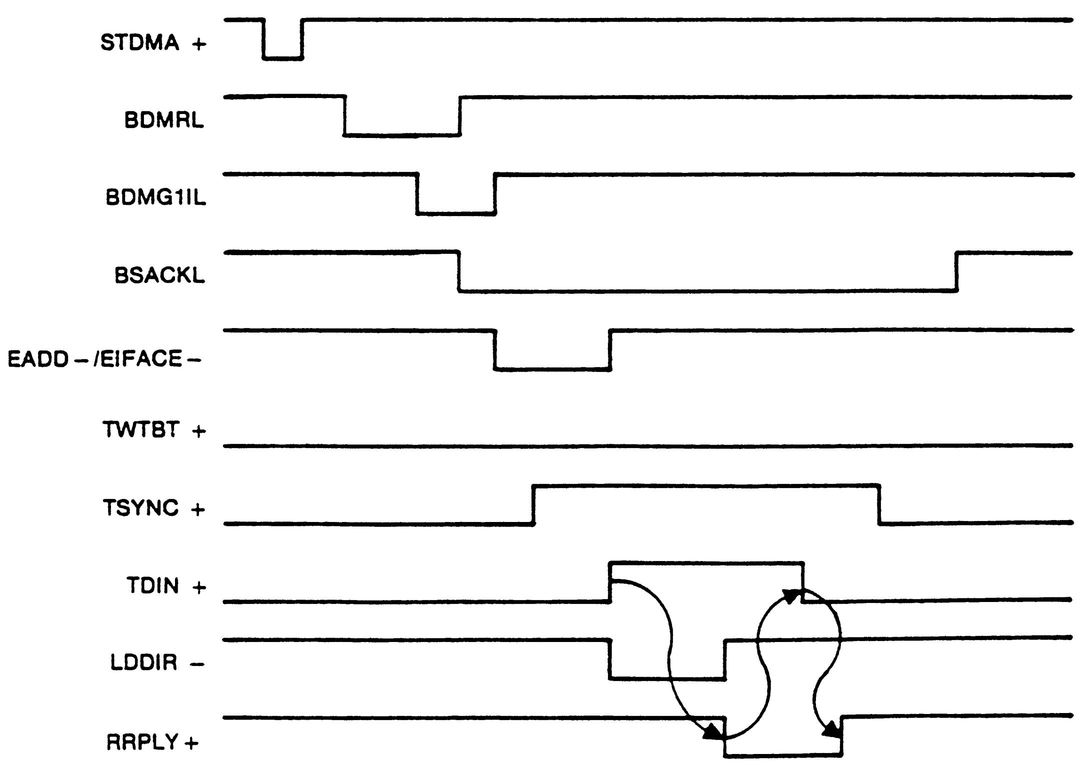


Figure 5-5. Q Bus DATI Transfer (Coupler as Bus Master)

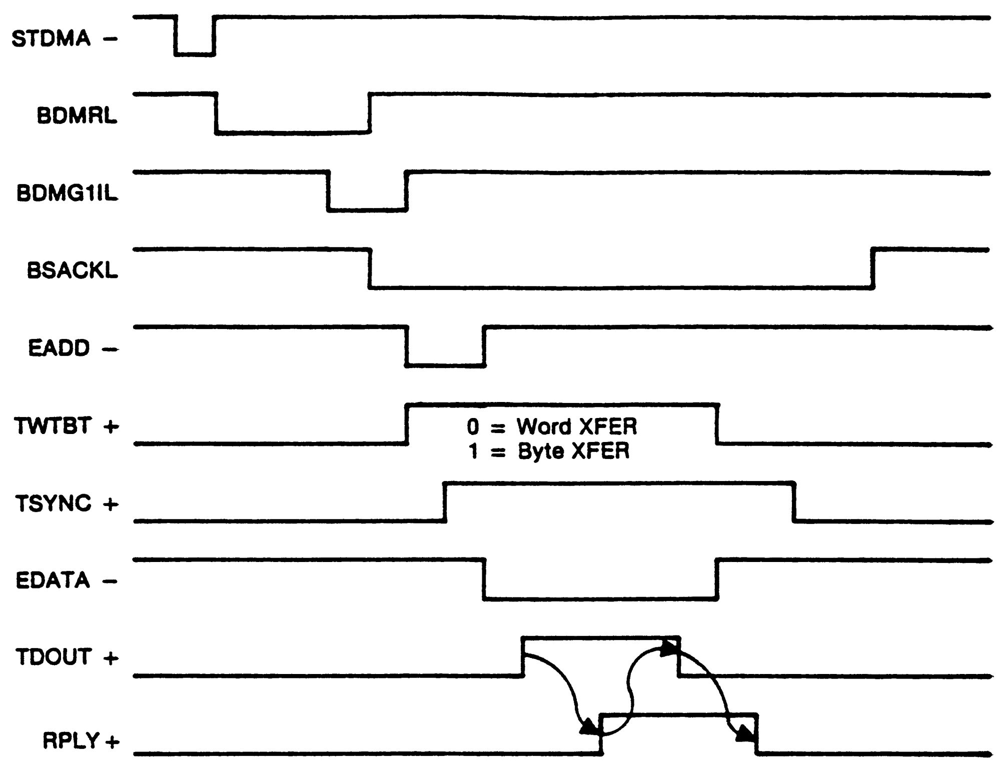


Figure 5-6. Q Bus DATO Transfer (Coupler as Bus Master)

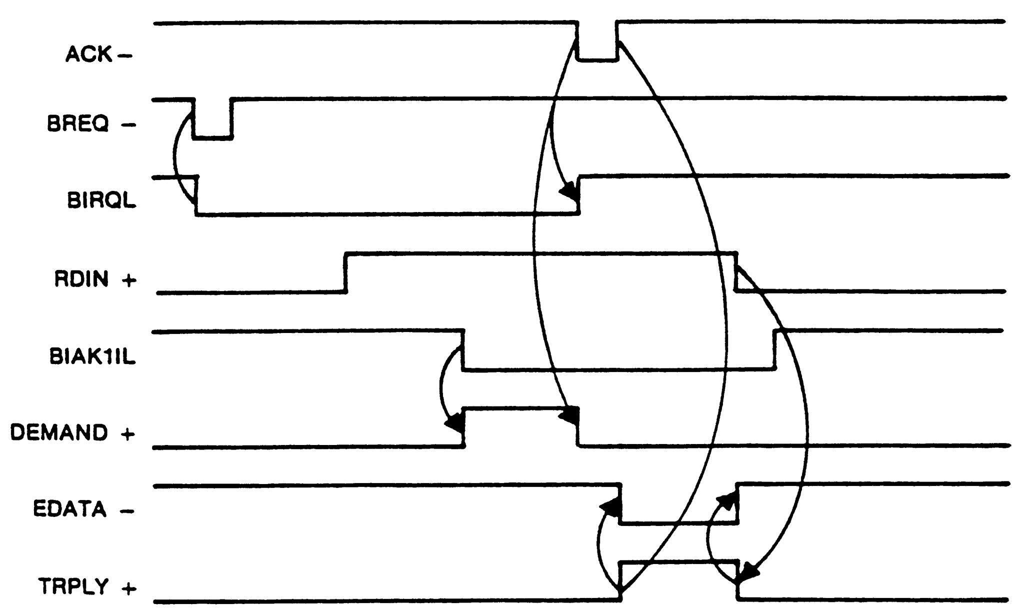


Figure 5-7. Interrupt Vector Transfer

Microprocessor Elements

The microprocessor comprises the following major elements:

A. 256 x 8 RAM

B. 512 x 8 ROM

C. Condition code and bit test multiplexers

D. 8-bit Arithmetic and Logic Unit (ALU)

E. 1K x 56-bit control store PROM

F. 2910 address sequencer

G. Vector register

H. Source, destination, and control pulse decode logic

These elements are interconnected to form the "brain" of the controller. Information is transferred among the elements over internal tri-state buses (the Y and the D-buses.).

A microprocessor functions under control of instructions stored in the control store. These instructions are called microinstructions because most often a series of them is required to perform a function. All of the microinstructions are called firmware, since once stored in the PROM, they cannot be altered. To understand the function of a microprocessor, please refer to "The Microprogramming Handbook" from Advanced Micro Devices, Inc., 901 Thompson Place, Sunnyvale, California 94086. Detailed technical descriptions of the 2901 four-bit, bipolar microprocessor slice and of the 2910 sequencer are given in Advanced Micro Devices "AM2900 Family Data Book." These two elements are the major components of the controller.

256 x 8 RAM (Sheet 14)

This RAM is the dynamic storage section of the coupler. Table 5-3 shows the contents of the RAM. The first 16 locations are reserved for the TSBA and TSSR register contents for each of the four logical units that can be connected to the coupler.

Also located in the RAM are the TSDBX registers, DMA DATA buffer and a context buffer for each of the four possible logical units. Each context buffer, shown in Table 5-4, contains internal drive status and an area reserved for assembling message packets.

Address register/counter 6E and 7E controls the RAM address lines. The starting address of the section of RAM to be written/read is loaded into the address register from the Y Bus by LXRE−. Signal INCRAM increments the RAM address.

The RAM consists of circuits 8E and 9E. The RAM data lines are connected to registers 10E and 10D.

Signal LXRF− writes the contents of the Y Bus into the addressed RAM location. Signal XSDF− gates the contents of the addressed RAM location to the D Bus.

Table 5-3. 256 x 8 RAM Contents

RAM Address (Hex)	Register	Unit	Bytes
00 L* 01 H	TSBA	0	16 Bytes
02 L 03 H	TSSR		
04 L 05 H	TSBA	1	
06 L 07 H	TSSR		
08 L 09 H	TSBA	2	
0A L 0B H	TSSR		
0C L 0D H	TSBA	3	
0E L 0F H	TSSR		
10 L 11 H 12 L 13 H 14 L 15 H 16 L 17 H	COMMAND PACKET		8 Bytes
23 27 2B 2F	TSDBX TSDBX TSDBX TSDBX	0 1 2 3	4 Bytes
30 37	DATA DMA BUFFER		8 Bytes
40 42	BLANK TAPE TIMEOUT COUNTER		3 Bytes
80-9C A0-BF C0-DF E0-FF	UNIT 0 CONTEXT UNIT 1 CONTEXT UNIT 2 CONTEXT UNIT 3 CONTEXT		32 Bytes 32 Bytes 32 Bytes 32 Bytes

*L = Low Byte, H = High Byte

Table 5-4. TSV05 Emulation Transport Context

			15 7	14 6	13 5	12 4	11 3	10 2	9 1	8 0	BIT POSITION
MESSAGE BUFFER ADDRESS	L	00	A7	A6	A5	A4	A3	A2	A1	A0	SET CHARACTERISTICS DATA
	H	01	A15	A14	A13	A12	A11	A10	A9	A8	
	EX	02			A21	A20	A19	A18	A17	A16	
		03									
LENGTH OF MESSAGE BUFFER	L	04									
	H	05									
CHARACTERISTICS MODE DATA		06	ESS	ENB	EAI	ERI					
		07									
EXTENDED FEATURES & BUFFERING CONTROL		08			HSP						
		09									
		0A									
		0B									
HEADER	L	0C									MESSAGE PACKET
	H	0D									
DATA FIELD LENGTH	L	0E									
	H	0F									
RBPCR	L	10									
	H	11									
XST0	L	12	MOT S	ONL S/1/3	IE S	VCK S/3	PED S	WLK S/3/6	BOT S/2/3	EOT S/2	
	H	13	TMK S/2	RLS 2	LET 2	RLL 2	WLE 3/6	NEF 3	ILS 3	ILS 3	
XST1	L	14							UNC 4	MTE 4	
	H	15	DLT 4							RBP 8	
XST2	L	16	XFS S								
	H	17	OPM S								
XST3	L	18		OPI 6	REV S		DCK S/6			RIB 2	
	H	19									
XST4	L	1A									
	H	1B									
		1C									
		1D									
		1E							DCK ST	EOT ST	INTERNAL STATUS
		1F	MBR	ONL ST	ATTNQ	VCK ST	RWDQ	RWDG	OLD REV	CMD WRT	

512 x 8-Bit ROM (Sheet 14)

ROM 11D is the "data look-up table" of the microprocessor. It contains constants and mask bits that permit rapid manipulation of tape subsystem information by the 2901 ALU. The tri-state ROM contents are typically used during A) command decoding, B) error logging, and C) command/interrupt queueing.

ROM address register 11E is loaded from the Y Bus by LXRD−. The contents of the addressed location are gated to the ROM D Bus by XSDE−. The self-test LED flip-flop is tied to the Table ROM to enable accessing the upper half of the ROM.

Controller Test Logic (Sheet 9)

The purpose of this logic is to perform conditional tests during conditional instructions and either enable or disable the CCE− input to the microsequencer. The eight conditions tested are gated to the CCE− output of test function multiplexer 2D by microcode field CR4-1 through CR4-3. The conditions tested for are:

A. Selected bits of the Y Bus

B. ALU = zero

C. ALU = non-zero

D. ALU carryout

E. ALU no carryout

F. CPU programmed I/O request or interrupt grant received (DEMAND+)

G. DMA cycle complete (DONE)

H. True condition to force "pass" state

Y-Bus bits to be tested are selected by field CR1-0 through CR1-2 which control multiplexer 4D. The selected bit is latched in register 2E by SCLK at the end of the instruction. Register 2E also stores the zero and carry output conditions of the ALU.

The flip-flops (3D) in both the DEMAND and DMA cycle DONE circuits guarantee that the external signals associated with these events are synchronized with the system clock.

The first five conditions must all be stored at the end of some prior instruction before being tested by a conditional instruction. Latch 2E stores these conditions at CR3-0 time. The last three conditions can be selected at any time.

2901B Microprocessor ALUs (Sheet 12)

The microprocessor ALUs comprise two AM2901B, four-bit, bipolar, microprocessor bit-slice integrated circuits connected in cascade to perform data manipulation on 8-bit bytes. A description of the operation of this device is given in the "AM2900 Family Data Book."

The D Bus supplies external data to the ALUs; output data from the ALUs is connected to the Y Bus. Control inputs to the ALUs are from the control store and are shown in Table 5-5. Table 5-6 lists the outputs of the ALUs.

Microsequencer (Sheet 10)

The microsequencer is an AM2910 microprogram control circuit described in "The AM2900 Family Data Book." It controls the sequence of execution of microinstructions stored in the control store.

Table 5-5. Control Inputs to 2901B ALU

ALU Mnemonic	Signal Source	Definition
A0-A3	Control Store	Address inputs to the A port of the 16-byte ALU memory.
B0-B3	Control Store	Address inputs to the B port of the 16-byte ALU memory.
I0-I8	Control Store	Instruction control lines: lines 0-2 select the data source to the ALU; lines 3-5 select the ALU function to be performed; lines 6-8 determine the destination of the output of the ALU (within the ALU) and the source of data supplied to the Y (output) bus.
CIN	Control Store	Carry input to ALU. Used during arithmetic operations. Can be forced O/I or Latched Carry Out from prior result.
CP	Crystal Oscillator	167 nanosecond clock to ALUs.

Table 5-6. 2901B ALU Outputs

Mnemonic	Definition
Zero+ (F=0)	Indicates result of ALU operation is Zero.
COUT+	Indicates a "carry out" of ALU.
RAM0	Least significant bit of RAM right/left shift multplexer.
RAM3	Most significant bit of RAM right/left shift multiplexer.
Q0, Q3	Q Register right/left shift ports.
Y0-Y7	8-bit output of ALU, Y0 is LSB.

Control store output address lines CSA0 through CSA9 select one of 1024 locations in the control store. Bits 4 through 7 of CR4 supply instruction codes to the microsequencer. Any one of 16 instructions can be selected, based on the pass/fail decision of the CCE− input. The conditional instructions select the next address to the control store. The primary sources of addresses are as follows:

A. The next sequential instruction (PC+1)

B. A counter/register within the microsequencer

C. A five-word LIFO stack within the microsequencer

D. Branch address directly from bits 0-7 of field five (CR5), CR4-0, and CR6-7

E. Microvector Address Register ID

Control Store (Sheet 11)

The control store contains the firmware instructions that control the operation of the coupler. It comprises seven 1024 x 8-bit Programmable Read Only Memories (PROMs) identified as 1A, 2A, 3A, 4A, 5A, 6A and 7A. The PROMs have a pipeline register at the output. The seven PROMs produce a 56-bit instruction word divided into seven 8-bit fields.

The contents of the control store are addressed by the microsequencer and strobed into the pipeline register by the SCLK− clock. The contents of the pipeline register (CR1-0/7 through CR6-0/7 and literal D00/07) are routed throughout the logic of the coupler.

Signal VEC+ disables the CR5 PROM outputs while the microvector address register is connected to the control processor. Signal XSDA− connects the contents of literal PROM 7A to the tri-state D Bus.

Microvector Address Register (Sheet 10)

This register is loaded with the contents of the Y Bus by signal LXRB−. If conditional testing makes the VEC output of the microsequencer True, the output of register ID supplants CR5 bits 0-7 as direct address inputs to the microsequencer. Note that VEC+ disables PROM 2A tri-state outputs.

Source, Destination, and Pulse Decode Logic (Sheet 13)

This logic comprises decoders enabled by bits of control registers CR6 and CR3 and the SCLK signal. The decoder outputs synchronize interaction of the various elements of the coupler.

Destination decoders 3E and 4E generate outputs that load registers with data from the ALU Y Bus. Source decoders 6B and 6C connect the outputs of registers to the ALU D Bus. The terms "source" and "destination" refer to the microprocessor ALUs: source of data to the ALU, destination of data from the ALU.

Control pulse decoder 18A generates pulses that initiate or terminate a function. The pulses primarily clock, direct set, or direct clear control flip-flops.

Note that the effect or function of each line of the registers is labeled on the logic drawing.

Peripheral Interface

The peripheral interface comprises the following logic sections:

A. Tape drive configuration switches and jumpers

B. Tape drive control, command, and status logic

C. FIFO data buffer controller

D. FIFO data buffer and tape drive data I/O logic drivers and receivers

Tape Drive Configuration Switches (Sheet 14)

Switch PAC 18B permits the operator to: A) select the floating vector addresses for logical units 1 through 3 (S1-S7), B) set Extended Features (Enable Address bits 10-21) (S8), and C) set the number of drives connected to the system (S9, S10, shown on Sheet 5). See Section 2 for a description of the switch settings.

The vector address switches are gated to the D Bus by buffer 17B by signal XSD9−.

Control, Command and Status Logic (Sheet 15)

This logic comprises registers that store the control (13B) and command (12B) signals to the tape drives and gate status signals from the drives to the D Bus (15B, 16B, 17E).

Signal LXR7 stores the contents of the Y Bus into 13B; LXR5 stores the contents of the Y Bus into 12B.

Tape drive status is gated to the D Bus during XSD7 and XSD8 and XSDD times. Transitory signals, such as file mark, hard or corrected error, end-of-tape mark, etc., are stored by latches 14B-13, 14B-7, 16C-9, and 16C-5.

The relationship among the control, command and status signals is described in the "Interface Description" section of the tape drive manual.

FIFO Controller (Sheet 16)

The FIFO controller supplies addresses and control signals to the FIFO data buffer. The FIFO is a buffer between the tape drive read/write data lines and the DMA buffer in the 256 x 8 RAM. All data between the CPU and tape drives passes through the FIFO and DMA buffers.

The FIFO controller logic is enabled by the ENAFIFO signal (flip-flop 10C-9). FIFO address circuit 7D is basically two 12-bit, wrap-around counters, used as pointers to produce the FAD0-FAD11 address lines to the FIFO RAM. The input-to-FIFO counter is advanced by S1; the output-from-FIFO counter is advanced by S0. After S1 is clocked, FIFWT− is asserted. After S0 is clocked,

FIFRD− is asserted. FIFWT− means "write data into FIFO from either tape or the Y Bus." FIFRD− means "read data from FIFO to either tape or the D Bus."

S-R latches are associated with the S0 and S1 inputs. Flip-flop 14B-9 and associated gates control S0; flip-flop 14B-4 and associated gates control S1.

When reading data from tape, signal FRSTR causes 14B-4 to set and S1 to advance the associated address counter and generate FIFWT−. LXR6− sets 14B-4 when the FIFO is loaded from the DMA data buffer. 14E-4 is cleared by FIFWT− delayed by C8 and R6.

14B-9 is set by either FDWDS (write to tape) or XSD4− and SCLK− (write to DMA data buffer). FIFRD− delayed by C7 and R5 clears 14B-9.

Conditions OUTACT+, INACT+, FULL+, EMPTY+, and DATLAT− are FIFO status signals gated to the D Bus for monitoring by the microprocessor.

Note that the S1 and S0 inputs are enabled after the trailing edge of the clock signals to the latches.

The Data Late (DATLAT−) signal is generated if either 12C-5 or 12C-9 set. These flip-flops set if either write or read strobes are too close together.

FIFO Data Buffer (Sheet 17)

The 4096 x 8-bit FIFO (8C and 7C) buffers all data between the tape drive and the DMA buffer in the 256 x 8 microprocessor RAM (see Note 1).

Circuit 9C is a parity generator/checker. Odd parity is generated to the output buffers; if even parity is detected at the input of the FIFO, PARER+ flip-flop 11C-9 sets. Signal FIFRD− flip-flop 11C-5, causing odd parity to be generated during data transfers to tape. During this time, the PARER+ flip-flop is disabled.

The following sequence occurs during data transfers to tape:

A. ENAFIFO+ signal asserted;
B. LXR6− clocks Y-Bus data from the DMA RAM into register 9B and clocks S1 input of FIFO controller 7D;
C. FIFWT− enables 9B tri-state outputs to FIFO data lines and writes data into the location addressed by FAD0-9;
D. Sequences B through C repeat until the sequence is terminated.
E. Before the preceding sequence, signal FG0 was issued to the addressed tape drive. Tape motion was started and, after tape is up to speed (FDBY asserted), FDWDS strobe is received.
F. FDWDS clocks S0 input of FIFO controller 7D.
G. Address lines FAD0-FAD11 select the first FIFO location that had been loaded with data.
H. Trailing edge of FIFRD− clocks FIFO data into register 8B and clocks parity bit flip-flop 11C-5.
I. FIFO input/output transfers continue concurrently (see note 2) until: 1) word count is zero, which terminates input transfers and 2) EMPTY+ is detected, which terminates output transfers.

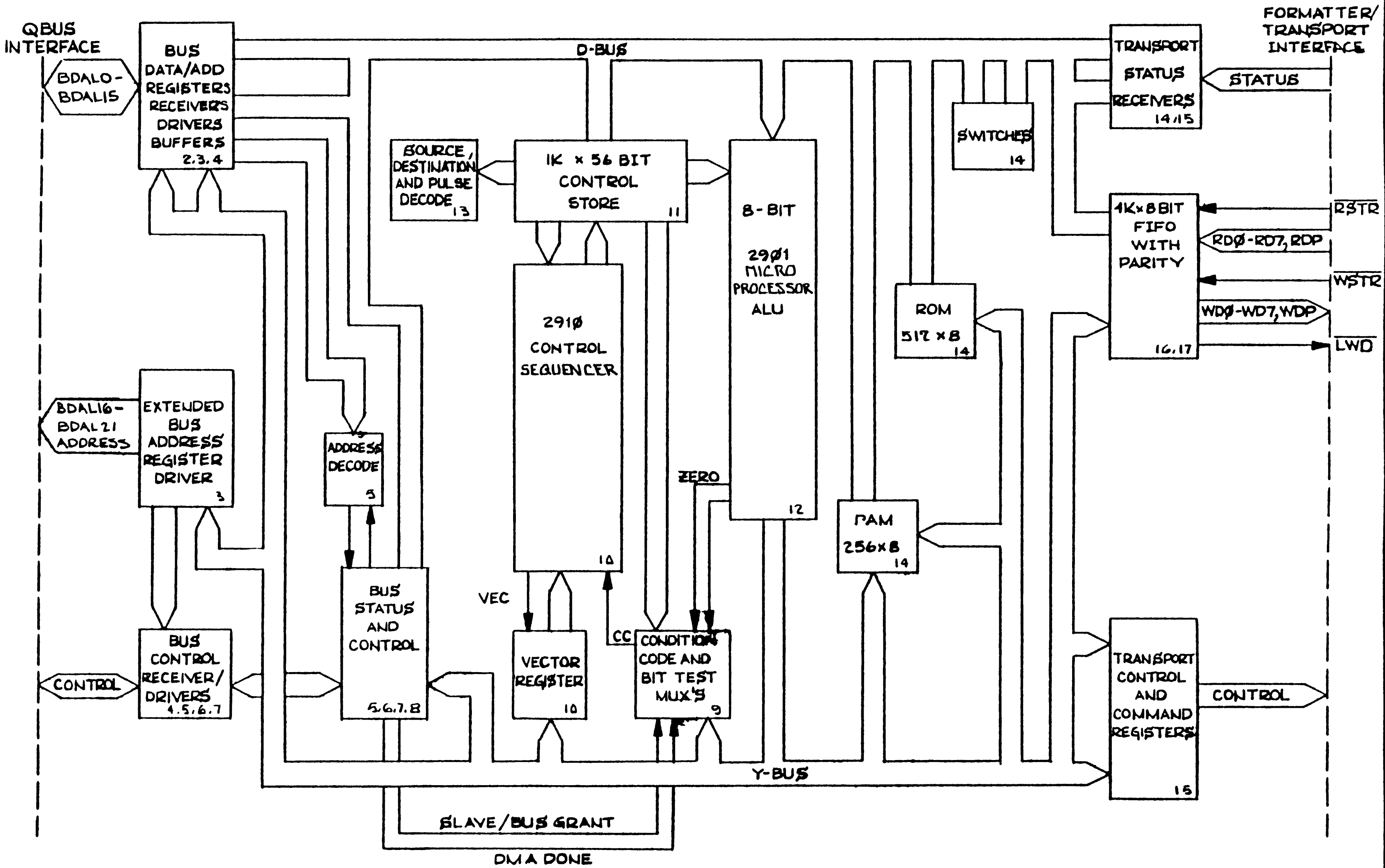
Notes

1. The total data buffer size in the coupler is actually 4106 bytes: 4096 byte FIFO buffer, input and output FIFO registers, and an eight-byte buffer in the 256 x 8 RAM.
2. The FIFO input and output transfers are asynchronous with respect to each other. Transfers appear to be able to occur simultaneously as far as the 2910/2901 microsequencer and tape interface are concerned. However, FIFO controller 15C treats its SI and SO inputs as "requests for transfers" and sorts them out internally to allow only one transfer at a time, in case SI and SO occur simultaneously.

   Controller 15C does this by selecting only one of the requests for service, gating the associated internal address counter to the FAD0-11 address lines, and responding with the appropriate FIFWT− or FIFRD− pulse. To complete the transfer, the internal address counter is advanced and the 19C flip-flop that triggered the SI or SO input is cleared.

   The basic system criteria is that the FIFO must always "stay ahead" of the tape interface during data transfers. Therefore, when reading tape, FIFO data must be transferred into computer memory faster than data is being received from tape. If not, the FIFO will fill up and overflow. When writing to tape, data must be supplied to the FIFO from computer memory faster than it is being written to tape. If not, the FIFO will empty too soon and underflow. Overflow or underflow will cause the data late (DATLAT−) error status to be generated.

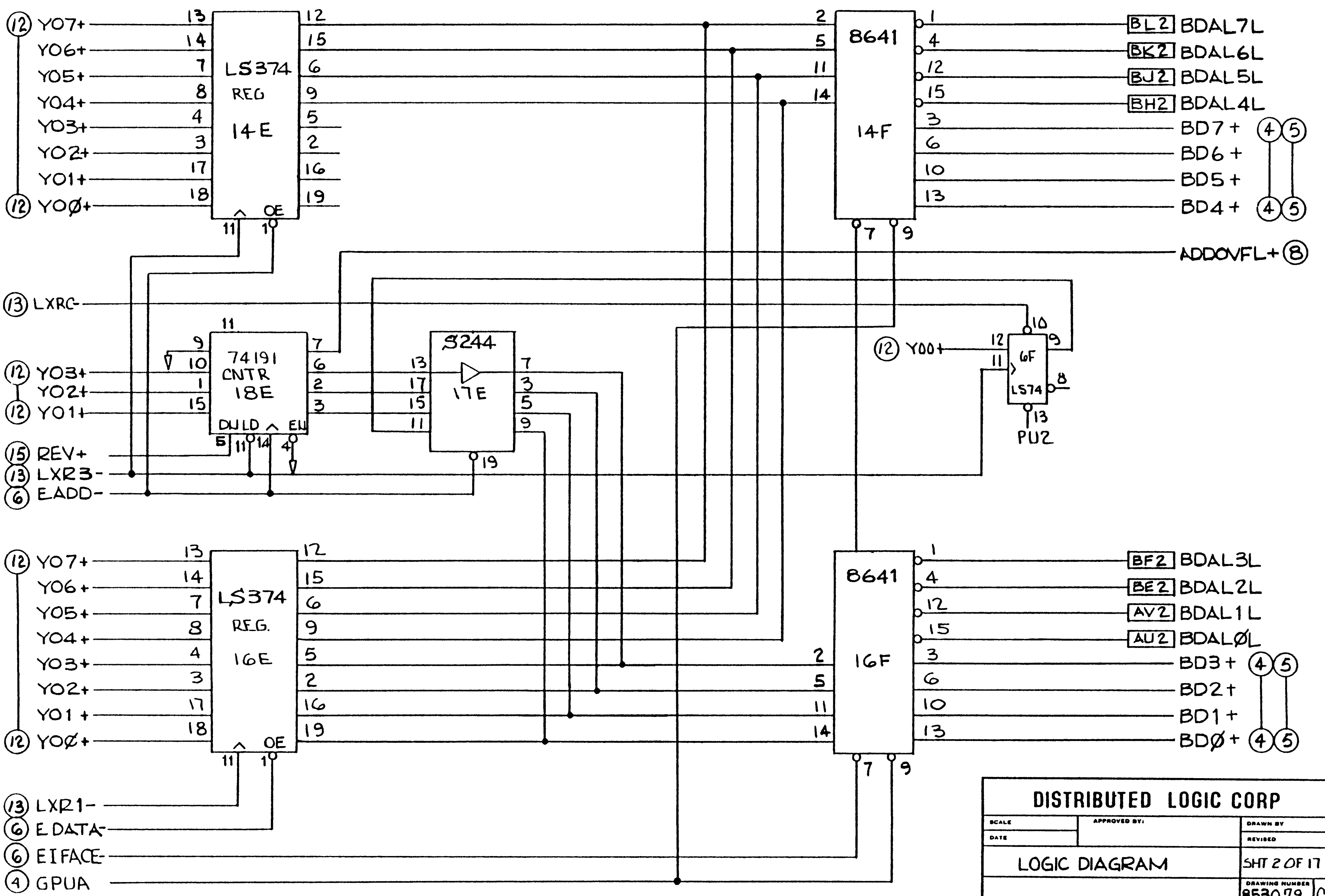
During data transfers from tape, RSTR− strobes tape data into register 10B. WRT+ is false in the read mode. Therefore, the output of 9B is disabled and the output of 10B is connected to the FIFO data lines and written into FIFO by FIFWT−. The addressed contents of the FIFO are connected to the D-Bus lines by XSD4− after register 7B is loaded with FIFO data by FIFRD−.



DISTRIBUTED LOGIC CORP

SCALE	APPROVED BY: R. H. 1-16-86	DRAWN BY
DATE		REVISED
DQ 142	LOGIC DIAGRAM	SHT 1 OF 17
USED ON		DRAWING NUMBER 853079 C

LSB ADDRESS/DATA OUTPUT REGISTERS AND TRANSCEIVERS



DISTRIBUTED LOGIC CORP

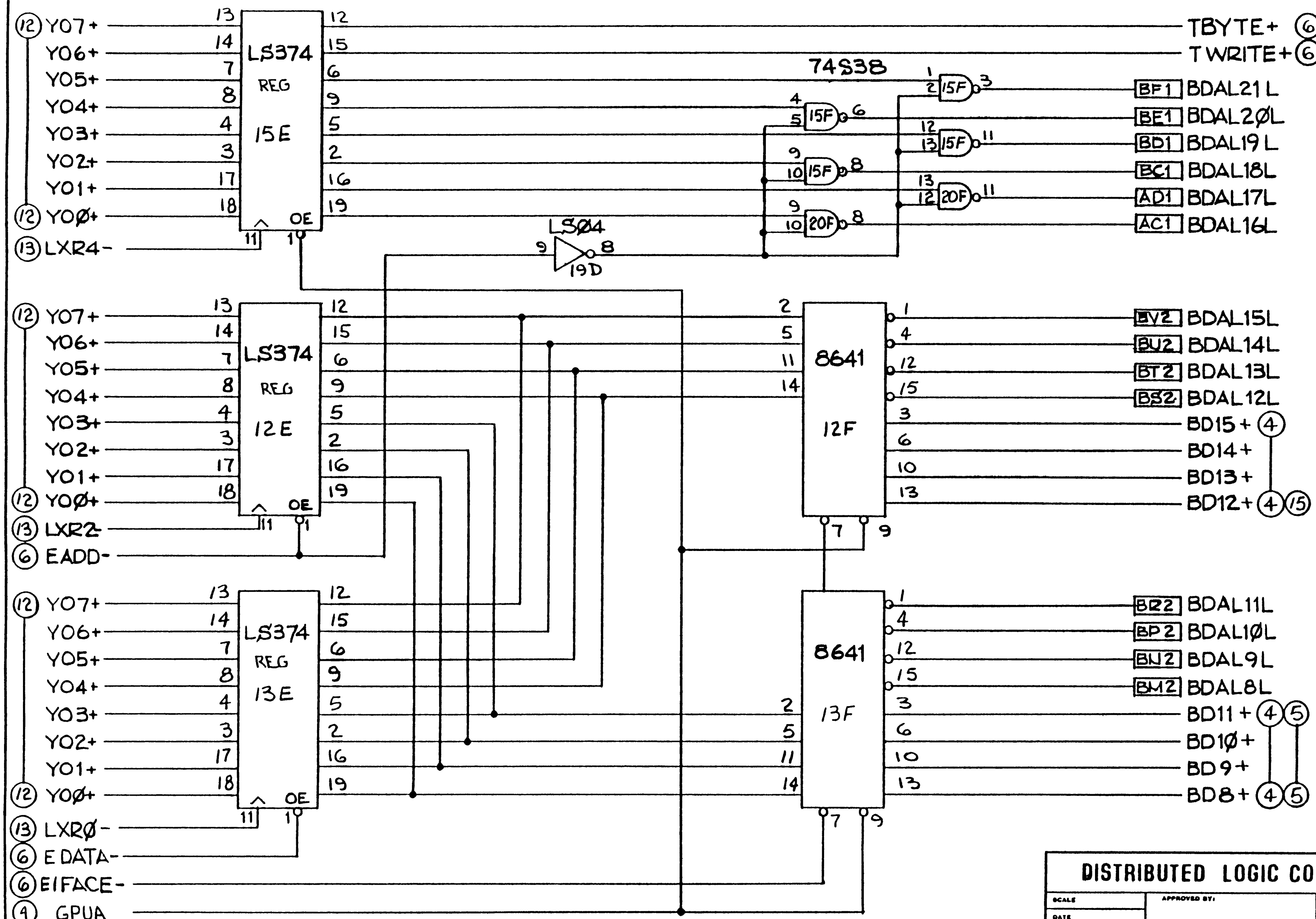
SCALE | APPROVED BY: | DRAWN BY
DATE | | REVISED

LOGIC DIAGRAM

SHT 2 OF 17

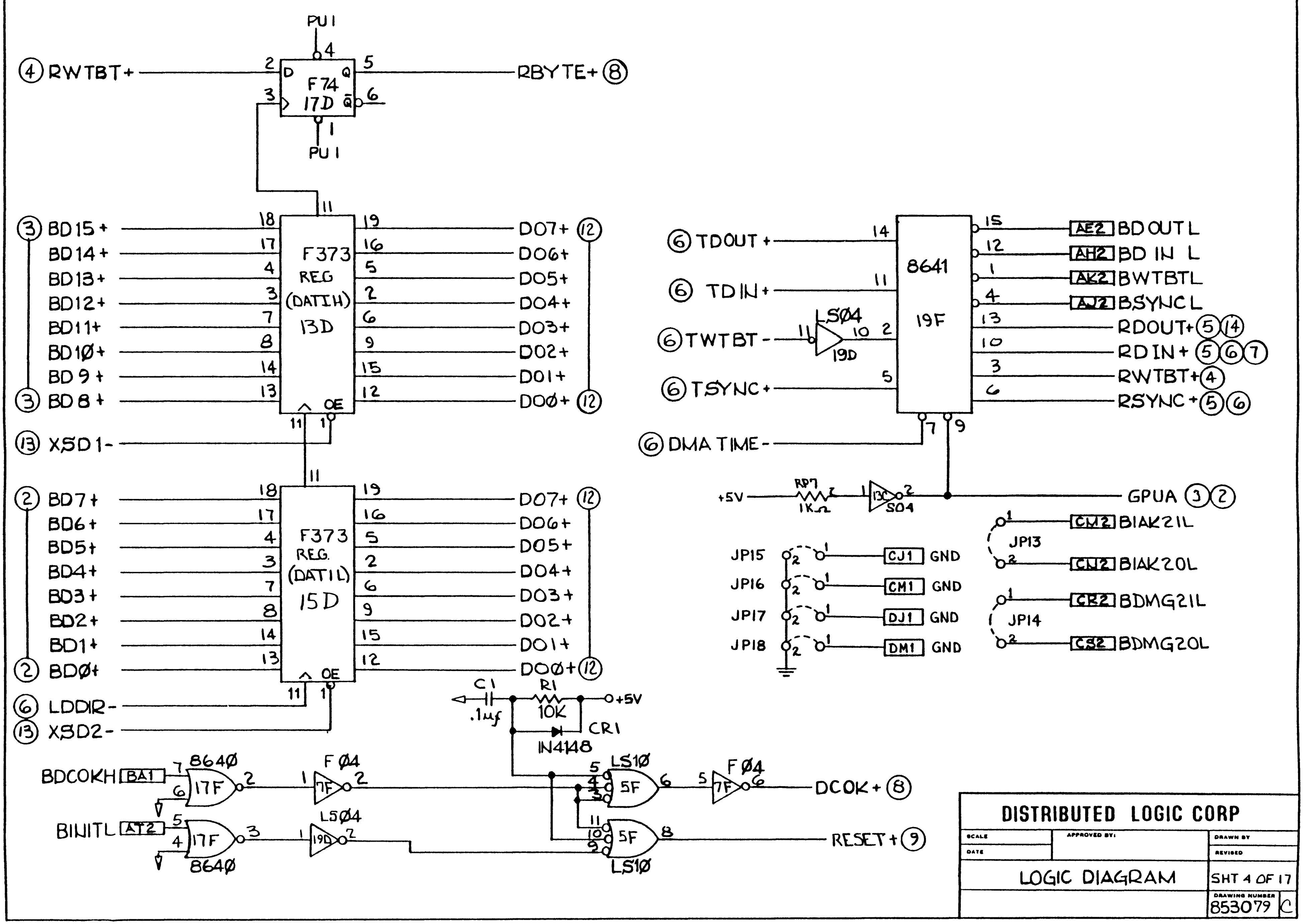
DRAWING NUMBER 853079 C

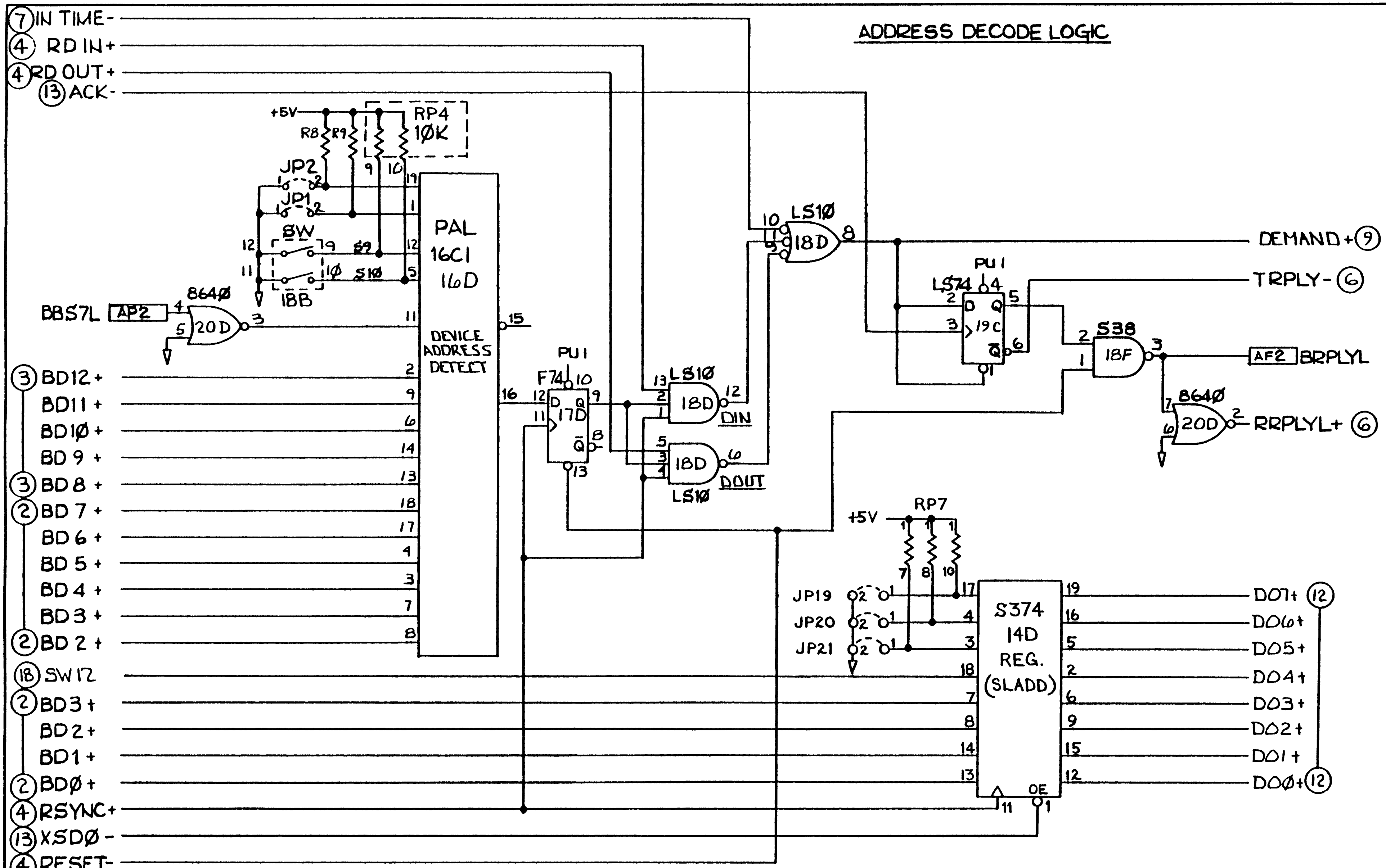
EXTENDED AND MSB ADDRESS/DATA OUTPUT REGISTERS AND TRANSCEIVERS



DISTRIBUTED LOGIC CORP		
SCALE / DATE	APPROVED BY:	DRAWN BY / REVISED
LOGIC DIAGRAM		SHT 3 OF 17
		DRAWING NUMBER 853079 C

DMA CONTROL TRANSCEIVERS AND DATA INPUT REGISTERS



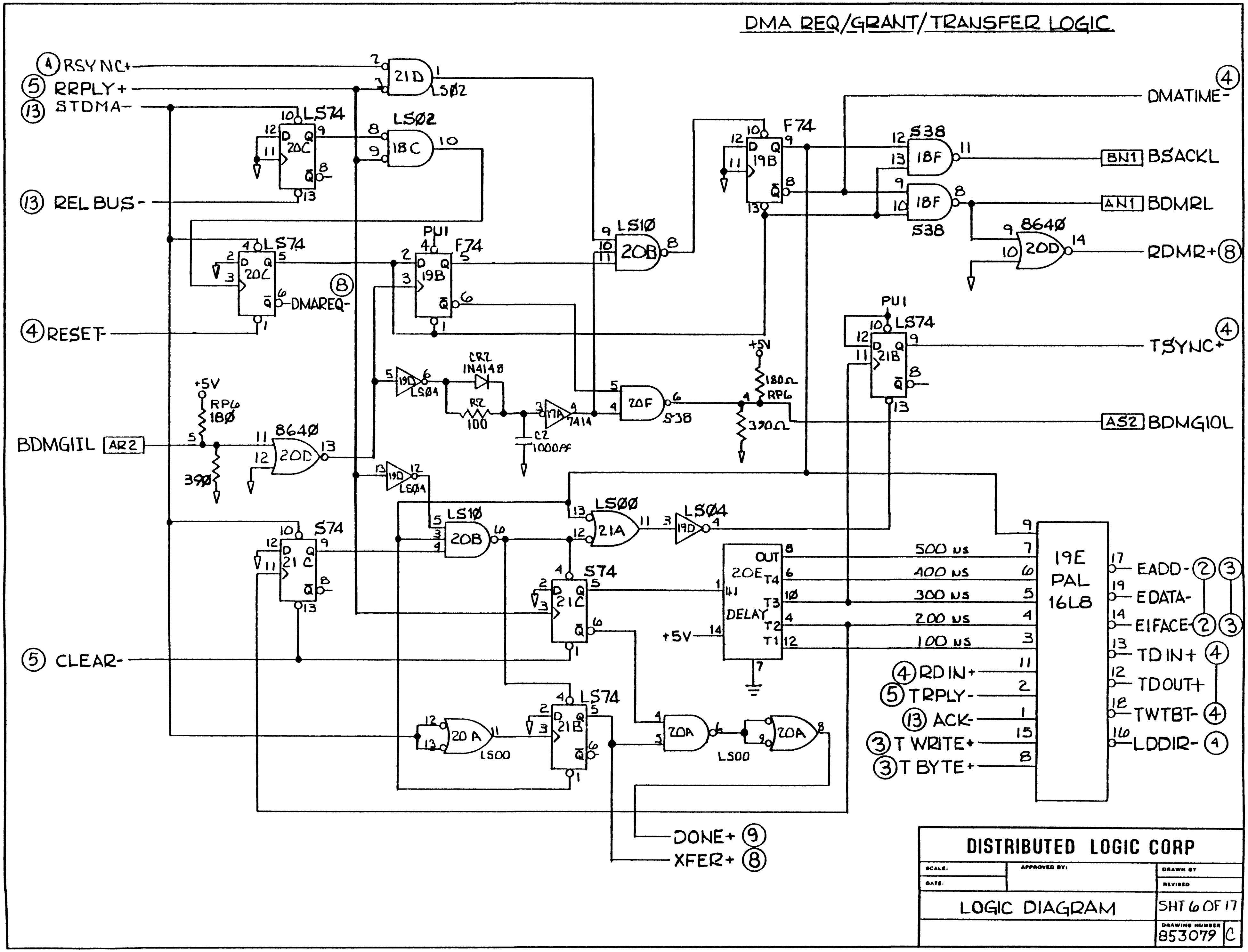


ADDRESS BLOCK	JUMPERS INSTALLED	
	JP1	JP2
772520 (DEFAULT)	YES	YES
772720	NO	YES
777360	YES	NO
777420 *	NO	NO

* ONLY 1 DRIVE PERMITTED IN THIS ADDRESS BLOCK

*LOGICAL UNITS	SWITCHES ON = Ø = CLOSED OFF = 1 = OPEN	
	S9	S10
1 (STD)	ON	ON
2	ON	OFF
3	OFF	ON
4	OFF	OFF

DISTRIBUTED LOGIC CORP		
SCALE:	APPROVED BY:	DRAWN BY
DATE		REVISED
LOGIC DIAGRAM		SHT 5 OF 17
		DRAWING NUMBER 853079 C


DMA REQ/GRANT/TRANSFER LOGIC
(4) RSYNC+
(5) RRPLY+
(13) STDMA-
(13) RELBUS-
(4) RESET-
BDMGIIL AR2
(5) CLEAR-
DMATIME- (4)
BN1 BSACKL
AN1 BDMRL
RDMR+ (8)
TSYNC+ (4)
AS2 BDMGIOL
DMAREQ- (8)
+5V
RP6 180
390
CR2 1N4148
R2 100
C2 1000pf
180Ω RP6
390Ω
21D LS02
LS74 20C
LS02 18C
LS74 20C
PU1 F74 19B
LS10 20B
F74 19B
S38 18F
S38 18F
8640 20D
8640 20D
19D LS04
17A 7414
20F S38
PU1 LS74 21B
19D LS04
LS10 20B
LS00 21A
LS04 19D
S74 21C
S74 21C
LS74 21B
20A LS00
20A
20A LS00
20E DELAY
OUT T4 T3 T2 T1
+5V
500 NS
400 NS
300 NS
200 NS
100 NS
19E PAL 16L8
EADD- (2) (3)
EDATA-
EIFACE- (2) (3)
TDIN+ (4)
TDOUT+
TWTBT- (4)
LDDIR- (4)
(4) RDIN+
(5) TRPLY-
(13) ACK-
(3) T WRITE+
(3) T BYTE+
DONE+ (9)
XFER+ (8)
DISTRIBUTED LOGIC CORP
SCALE:
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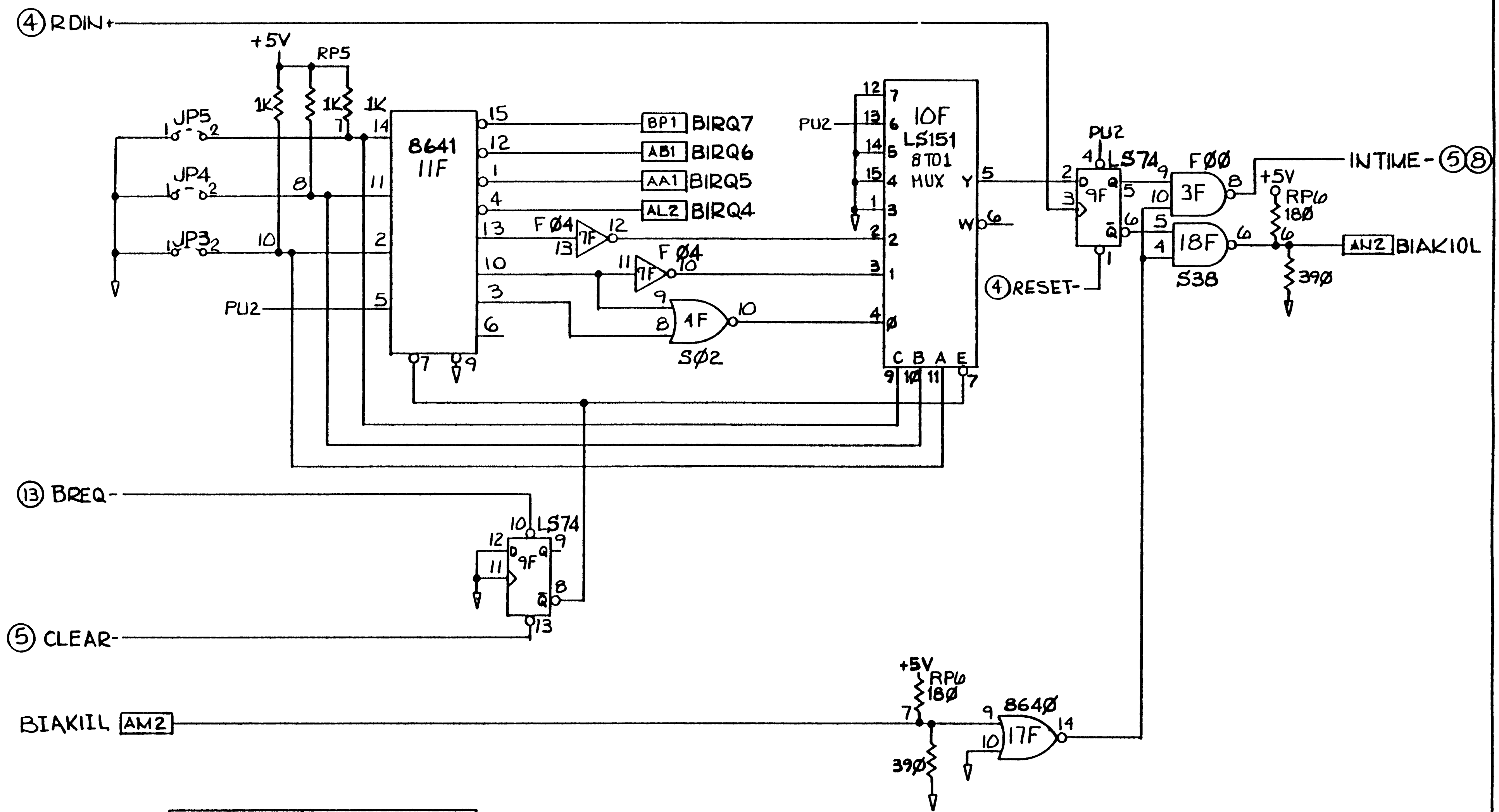
LOGIC DIAGRAM
SHT 6 OF 17
DRAWING NUMBER
853079 C

BUS REQ/GRANT LOGIC



BUS REQ PRIORITY LEVEL	JUMPERS INSTALLED		
	JP5	JP4	JP3
4 (DEFAULT)	YES	YES	YES
5	YES	YES	NO
6	YES	NO	YES
7	NO	NO	YES

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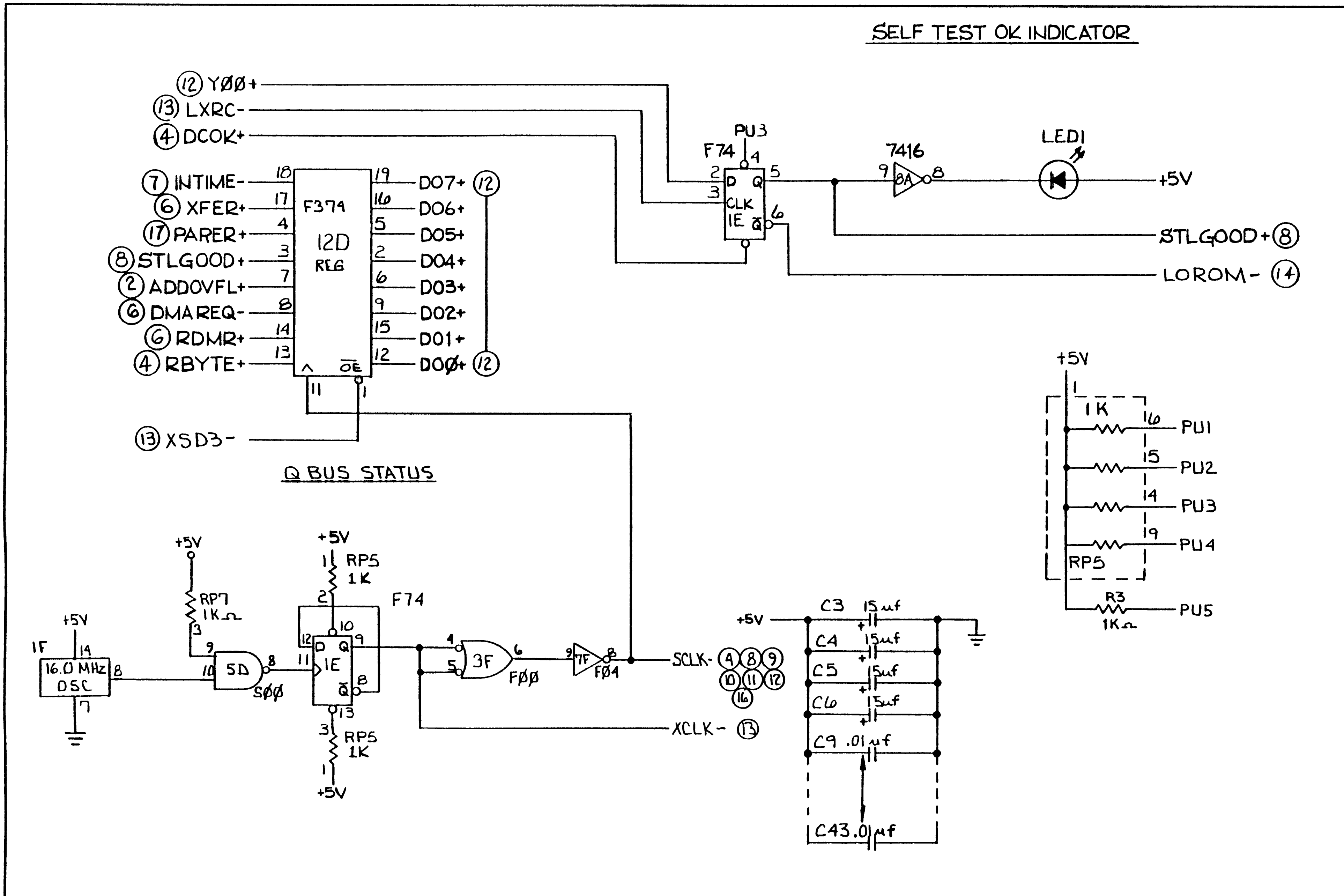
DATE:		REVISED
LOGIC DIAGRAM		SHT 7 OF 17
		DRAWING NUMBER 853079 C



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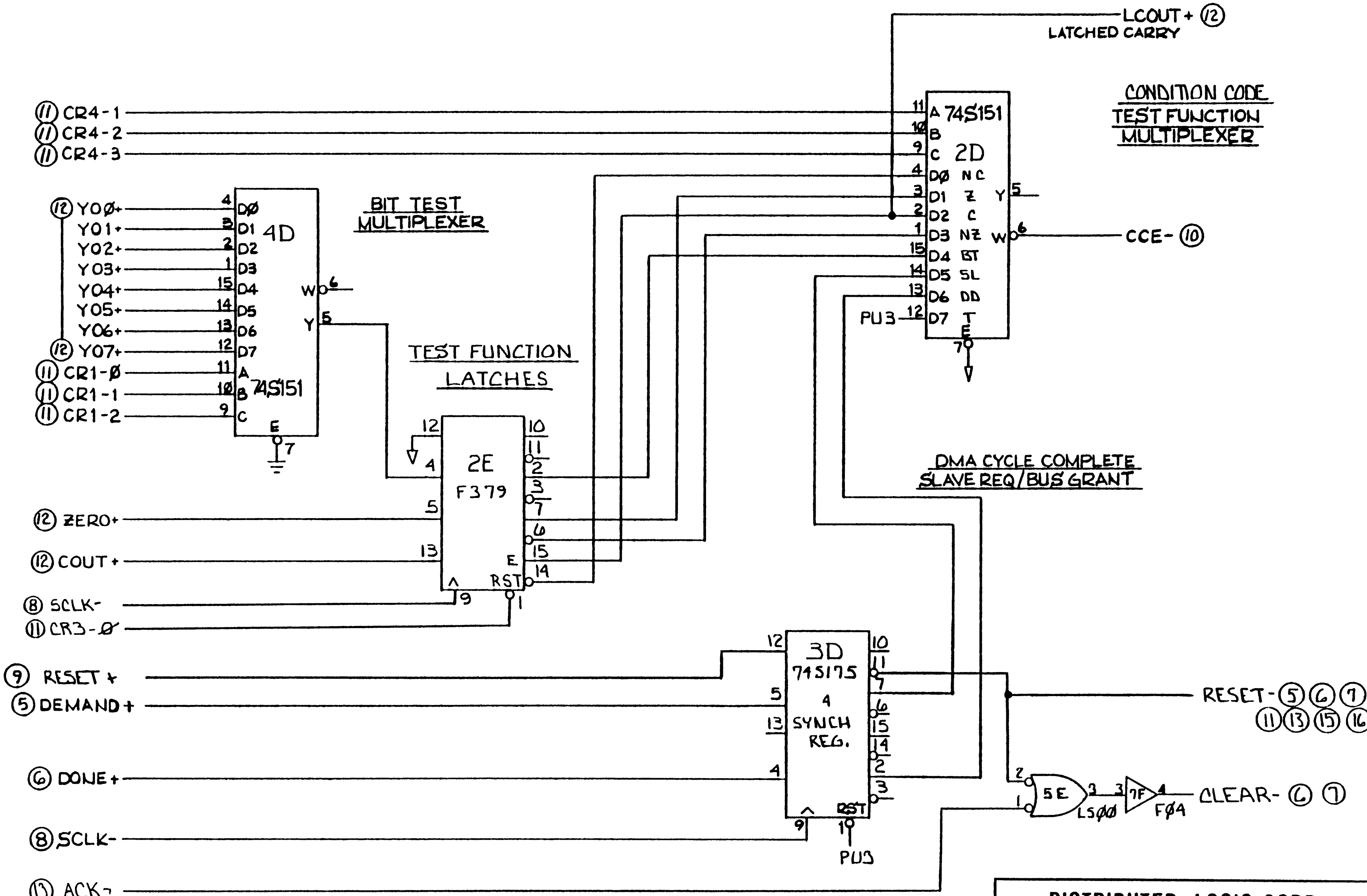
CONTROLLER TEST LOGIC



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LOGIC DIAGRAM		SHT 9 OF 17
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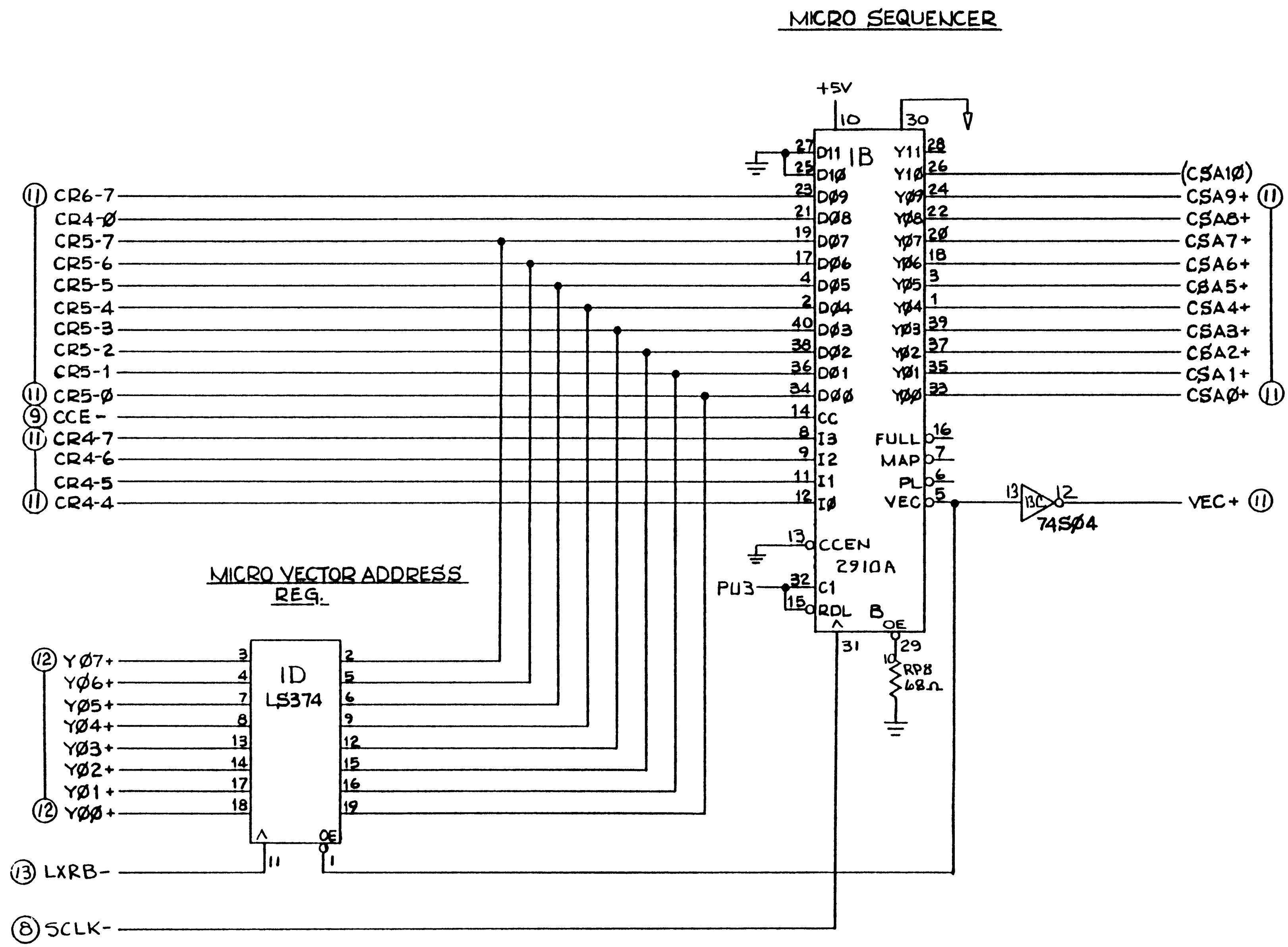

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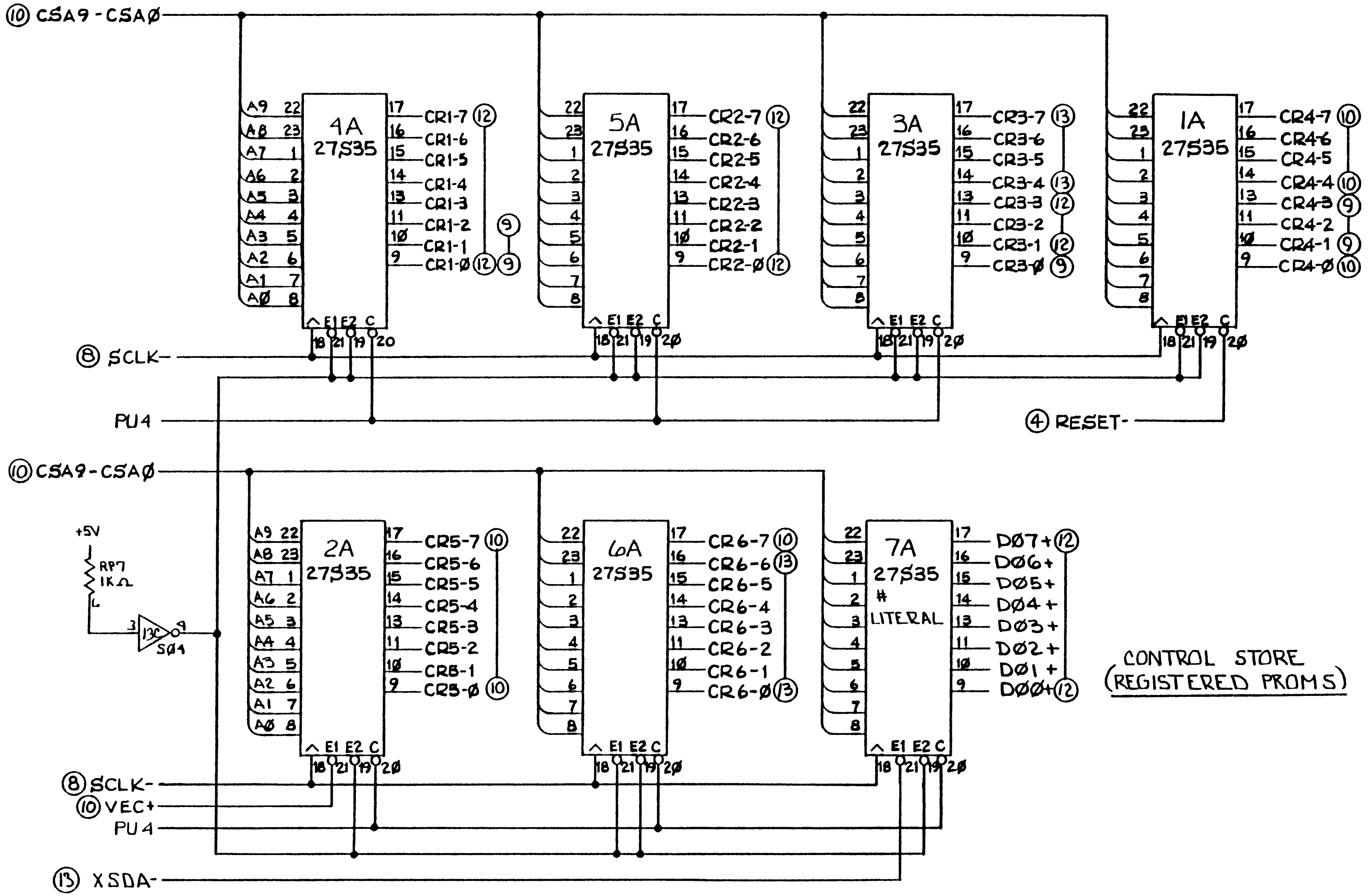
LOGIC DIAGRAM	SHT 10 OF 17
DRAWING NUMBER	853079 C



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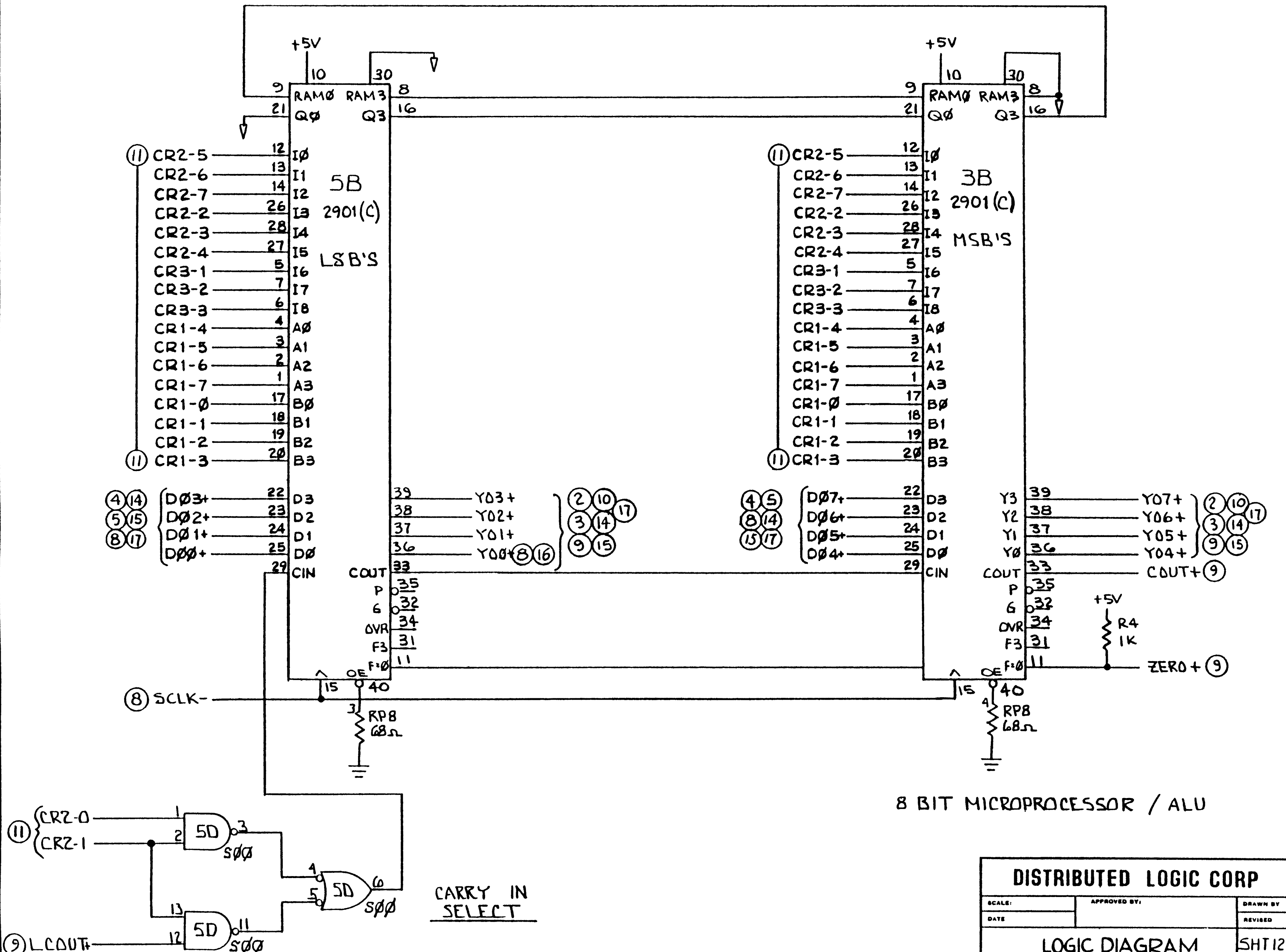
DATE		REVISED
	LOGIC DIAGRAM	SHT 11 OF 17
		DRAWING NUMBER 853079 C



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SCALE:	APPROVED BY:	DRAWN BY
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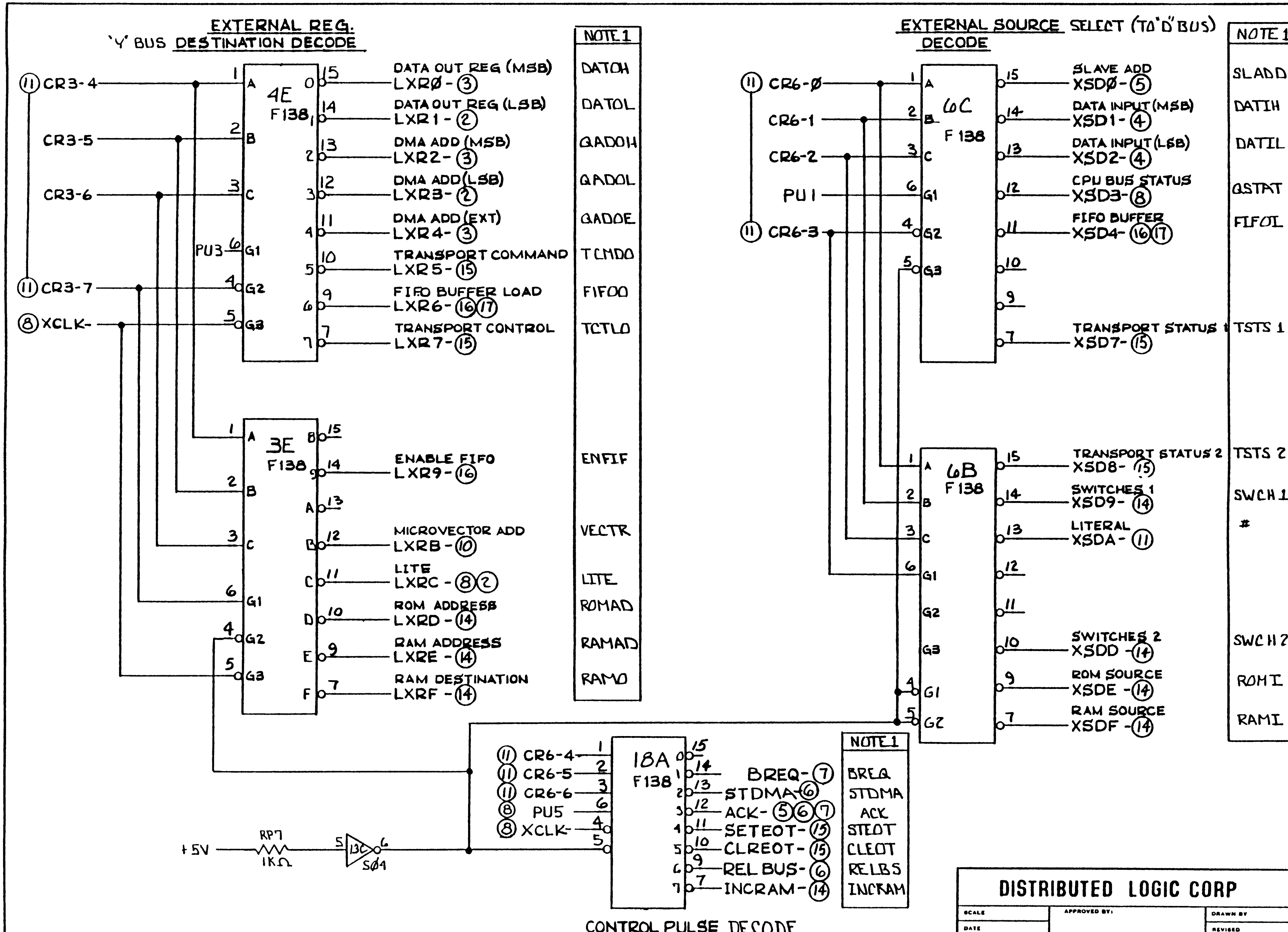
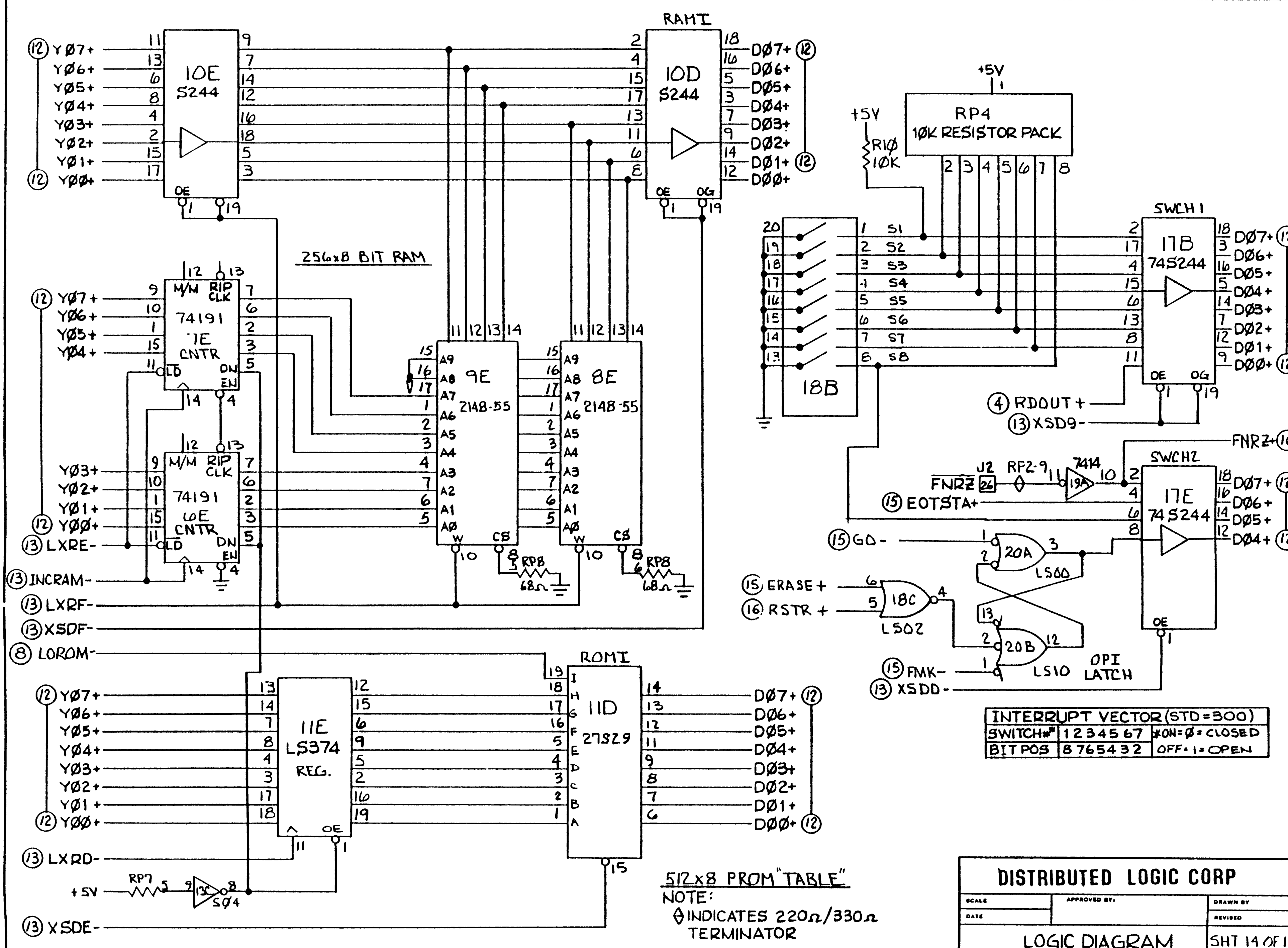
LOGIC DIAGRAM		SHT 12 OF 17
		DRAWING NUMBER 853079 C



1. MNEMONICS USED ON FIRMWARE LISTING.

NOTES: UNLESS OTHERWISE SPECIFIED

DISTRIBUTED LOGIC CORP		
SCALE	APPROVED BY:	DRAWN BY
DATE		REVISED
LOGIC DIAGRAM		SHT 13 OF 17
		DRAWING NUMBER 853079 C



INTERRUPT VECTOR (STD=300)		
SWITCH#	1 2 3 4 5 6 7	*ON=0=CLOSED
BIT POS	8 7 6 5 4 3 2	OFF=1=OPEN

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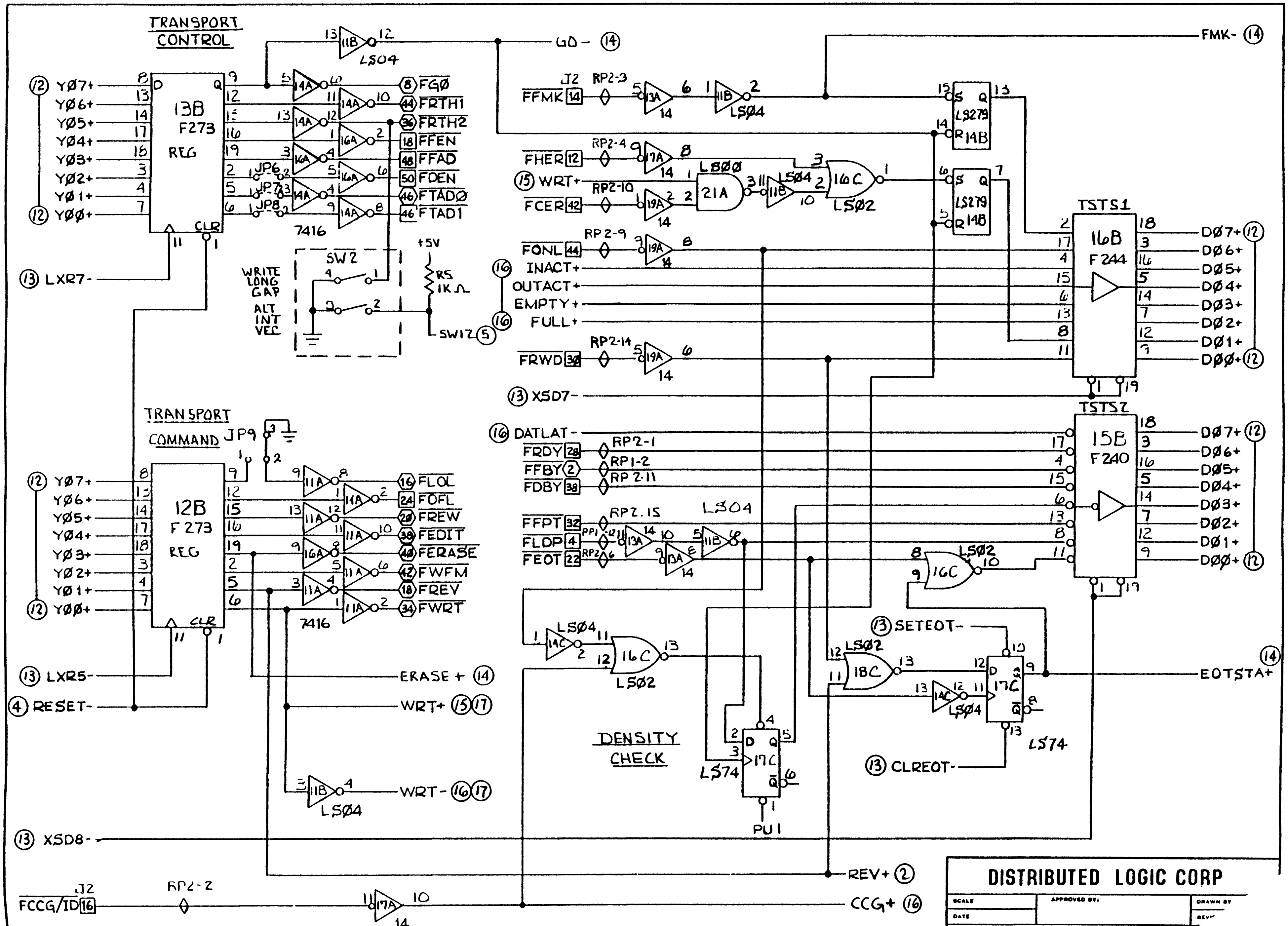
DATE | REVISED

LOGIC DIAGRAM

SHT 14 OF 17

DRAWING NUMBER 853079 C



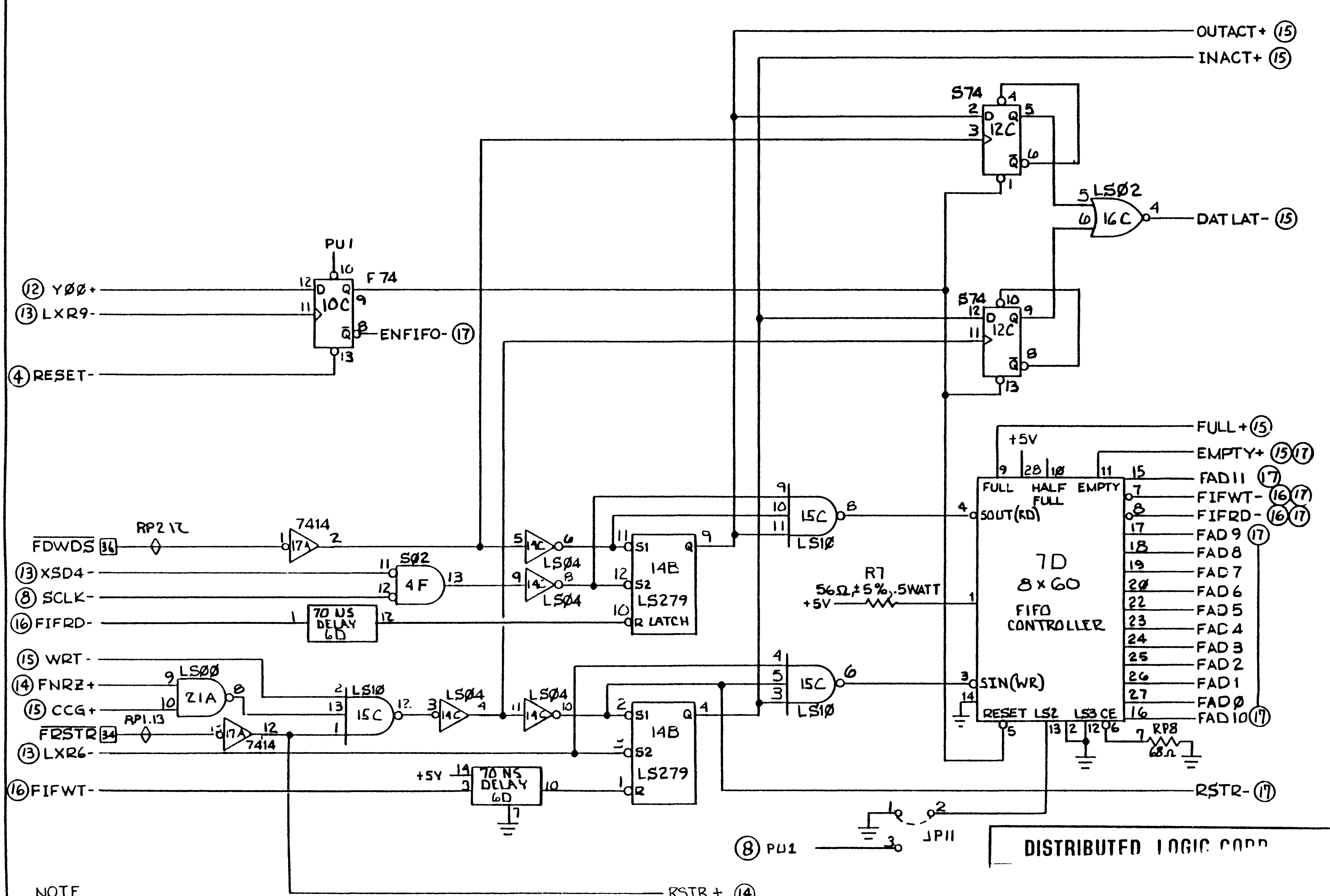
NOTE: ◇ INDICATES 220Ω/330Ω TERMINATOR.

DISTRIBUTED LOGIC CORP

SCALE	APPROVED BY:	DRAWN BY
DATE		REV

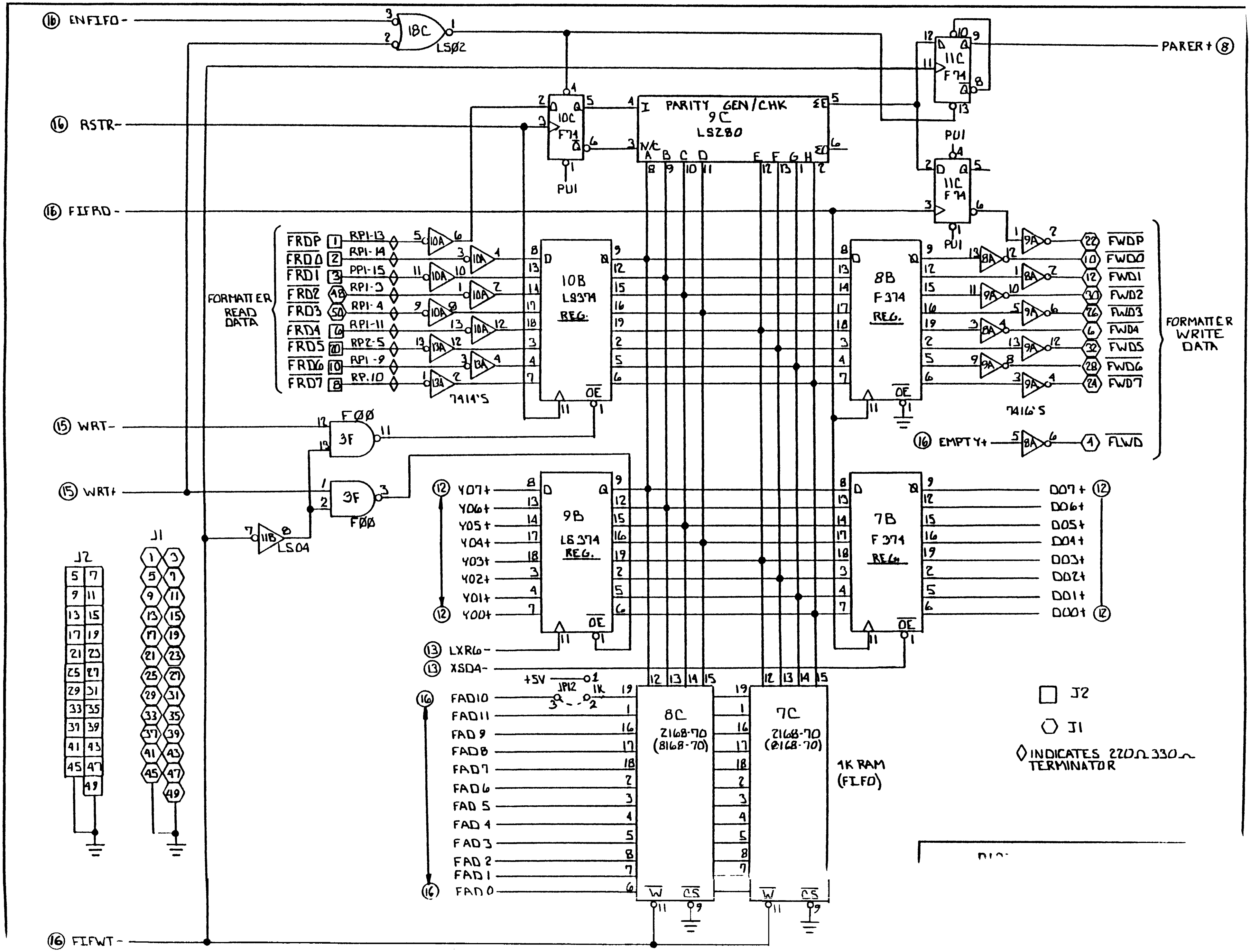
LOGIC DIAGRAM

FIFO CONTROLLER



NOTE
◊ INDICATES 220Ω/330Ω TERMINATOR

DISTRIBUTED LOGIC CORP



ENFIFO-
RSTR-
FIFRD-
WRT-
WRT+
FIFWT-
PARITY GEN/CHK
9C
LS280
10C
F74
11C
F74
18C
LS02
PU1
PARER+
FORMATTER READ DATA
FRDP
FRD0
FRD1
FRD2
FRD3
FRD4
FRD5
FRD6
FRD7
7414'S
10B
LS374
REG.
8B
F374
REG.
FORMATTER WRITE DATA
FWDP
FWD0
FWD1
FWD2
FWD3
FWD4
FWD5
FWD6
FWD7
7416'S
EMPTY+
FLWD
3F
F00
11B
LS04
9B
LS374
REG.
7B
F374
REG.
Y07+
Y06+
Y05+
Y04+
Y03+
Y02+
Y01+
Y00+
D07+
D06+
D05+
D04+
D03+
D02+
D01+
D00+
LXRG-
XSD4-
+5V
JP12
1K
FAD10
FAD11
FAD 9
FAD8
FAD7
FAD 6
FAD 5
FAD 4
FAD3
FAD 2
FAD 1
FAD 0
8C
2168-70
(8168-70)
7C
2168-70
(8168-70)
1K RAM
(FIFO)
J2
J1
INDICATES 220Ω 330Ω TERMINATOR

BLANK